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Advanced Transient Waveform Recording Techniques

by

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ILLUSTRATIONS

ADVANCED TRANSIENT WAVEFORM RECORDING TECHNIQUES

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Ralph E. Partridge

ABSTRACT

New techniques for transient waveform recording are required for situations where application of the conventional oscilloscope-camera combination approach is not feasible. This report studies the recording process in fundamental terms, indicates avenues to be explored, points out new devices and technologies which can be applied, and outlines progress made on this and related problems in the recent past.

I. INTRODUCTION

There are numerous requirements for recording transient electrical waveforms. In the field testing organization of the Los Alamos Scientific Laboratory, such requirements may arise in connection with measurements of the reaction history of an experimental nuclear device, for measuring the nuclear outputs of such devices, for nuclear effects studies, and in connection with various fundamental physics experiments. The conventional instrument for making a permanent record of a transient electrical waveform is the oscilloscope-camera combination. More and more frequently, however, there arise situations in which it is not feasible to apply this technique. For instance, in a rocket-borne instrument such considerations as size, weight, power consumption, and film recovery preclude use of this approach. Alternatively, the high-frequency attenuation and phase distortion of the long runs of coaxial cable required for measurements at underground sites would make it desirable to have an expendable instrument which could be placed downhole and would store, process, and telemeter up the data at a reduced rate over less expensive signal lines. Measurements to be made beneath the surface of the ocean can present problems related to both of the foregoing situations. Observations made in less hostile environments such as in an aircraft or even in the laboratory may sometimes be considerably increased in value by having the data immediately available in a computer-compatible format rather than as a film record.

This report is concerned with alternatives to the oscilloscope-camera combination. The minimum analog data bandwidth to be considered is of the order of 50 MHz, and there is a real need for bandwidths up to 1 GHz. To be deemed worthy of study, the systems of interest should have at least the same resolution as an oscilloscope, and hence should be able to resolve between 100 and 1000 points (tracewidths) on the signal axis, and between 200 and an unlimited number of points on the time axis. Linearity should be commensurate with resolution (through calibration if need be).

Throughout most of this discussion, we shall not be describing the present state of the art, but rather, we wish to scrutinize what conceivably could become feasible through in-house or outside development in the next one to three years. This discussion involves a family of instruments, rather than one particular set of specifications. There is an area of application for any portion of this family.

Some versions of the recording system must be highly radiation resistant. Other versions must be capable of storing the data for many seconds or minutes and then telemetering it out--as for example in a rocket which will have telemetry blackout problems, while still others must be capable of telemetering out the data within milliseconds--as for example from a detonation underground , before arrival of the hydrodynamic shock. Most versions must present the final data in digital form on magnetic tape or punched cards without the need for intermediate data handling such as film reading and calibration. One class must be sufficiently inexpensive to be expendable, while others could be extensive laboratory or field installations. Low power consumption is a highly desirable feature of some types. Many measurements will require many parallel simultaneous recording channels.

II. FUNDAMENTAL CONSIDERATIONS IN TRANSIENT WAVEFORM RECORDING

In order to study the possible applicability of all available physical phenomena to transient recording, we must first step back and take a broad-perspective look at the entire recording process, from the signal input to the final data form. We note that essentially all high speed transient waveform measurements require that a signal appearing on a coaxial cable should eventually be made available in a computer-compatible format for further processing in a central computer facility. Thus, the intermediate recording steps essentially amount to a hierarchy of progressively less and less volatile forms of storage, in progressively more computer-compatible forms. To devise an optimum recording system, then, it is desirable to minimize the number of these intervening steps and to maximize their reliability and accuracy, while minimizing their environmental limitations, volume, and power consumption. The conversion of a signal from a variation of voltage with respect to time into static computer input data implies (a) that at each point in time the analog voltage is sampled and converted into a digital (possibly binary) form, and (b) that data points separated in time become points separated in space , e.g., in separate cells in computer memory or in different locations on punched cards. We shall see eventually that this conversion from a sequence of points in time to a spatial separation is one of the most fundamental processes in transient waveform recording.

The recording techniques investigated or proposed in this report tend to fall naturally into two classes: those in which the conversion of time separation into spatial separation takes place at the input, followed by a subsequent analog-to-digital conversion of the signal voltage, and those in which these two conversions take place in the opposite sequence. The more difficult problems in designing a recording instrument tend to be associated with the first conversion to take place. The most general recording instrument will have three storage media: one in which the signal is stored before the first conversion takes place, a second (of different nature) where the data are stored between the two conversion processes, and a third where the data are in final digital form. Particular systems may have one or two of these storage media absent or not readily identifiable.

The conventional oscilloscope-camera arrangement fits readily into this description. The first analog storage medium, whose significance is frequently overlooked in discussions of the recording process, is ordinarily a coaxial delay line used to store the transient waveform until such time as the deflection and writing circuitry have been triggered and are ready to accept a signal. The initial conversion of the incoming signal into a two-dimensional display on the phosphor screen provides the time-spatial separation conversion, a portion of the amplitude conversion, and storage. Through the photographic process this temporary storage in the form of a decaying excitation is converted to a more permanent form in the film emulsion. The subsequent reading of the film converts the data from an analog to a digital format and presents the computer with a matrix of amplitude and time data points.

III. PROMISING RECORDING SYSTEM APPROACHES

The first of the abovementioned two alternative conversion sequences with their three interspersed storage media is illustrated in block diagram form in Fig. 1. Examples of existing and proposed recording system approaches which correspond to this concept are shown in Figs. 2 through 8 and are

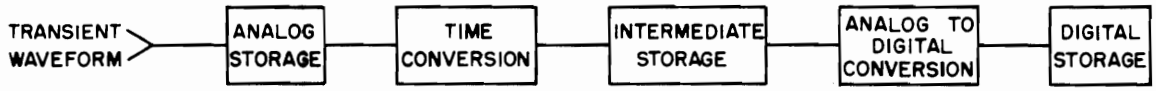


Fig. 1. Block diagram—time conversion preceding amplitude conversion.

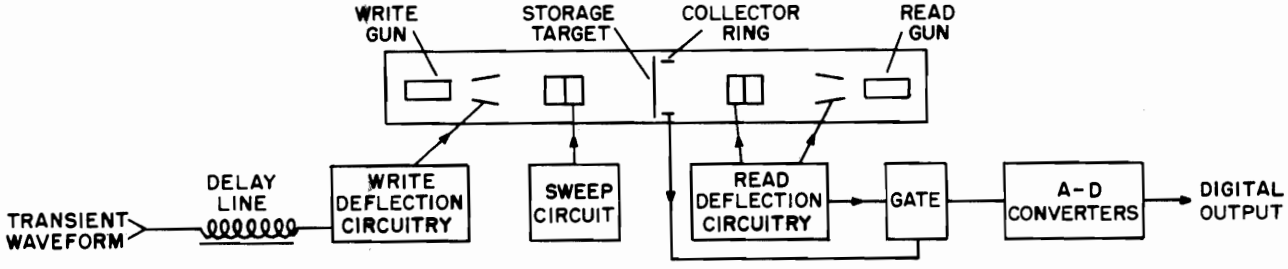


Fig. 2. The scan converter.

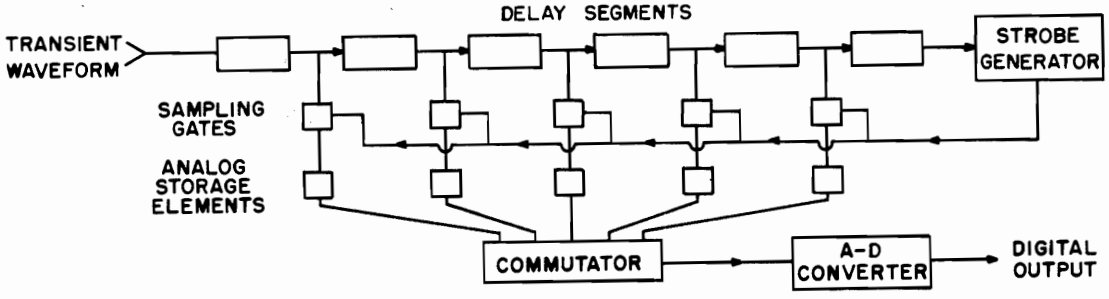


Fig. 3. Segmented delay medium.

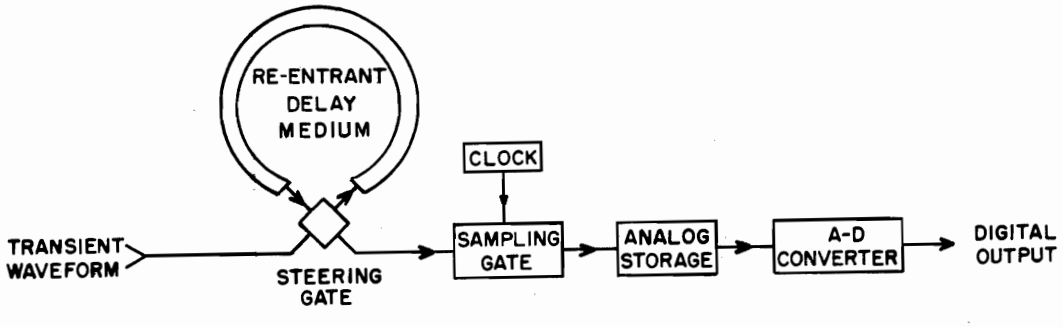


Fig. 4. Recirculating delay medium.

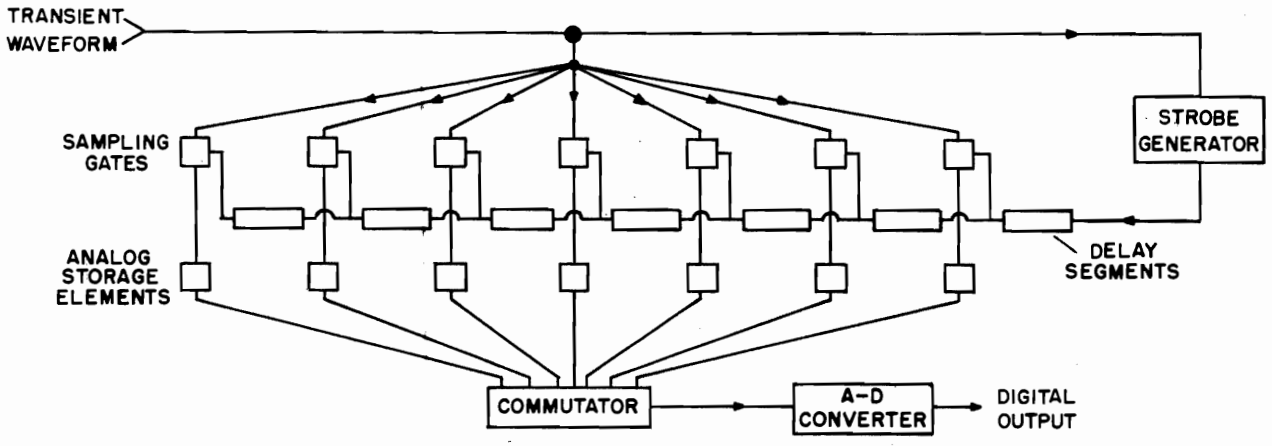


Fig. 5. The fanout approach.

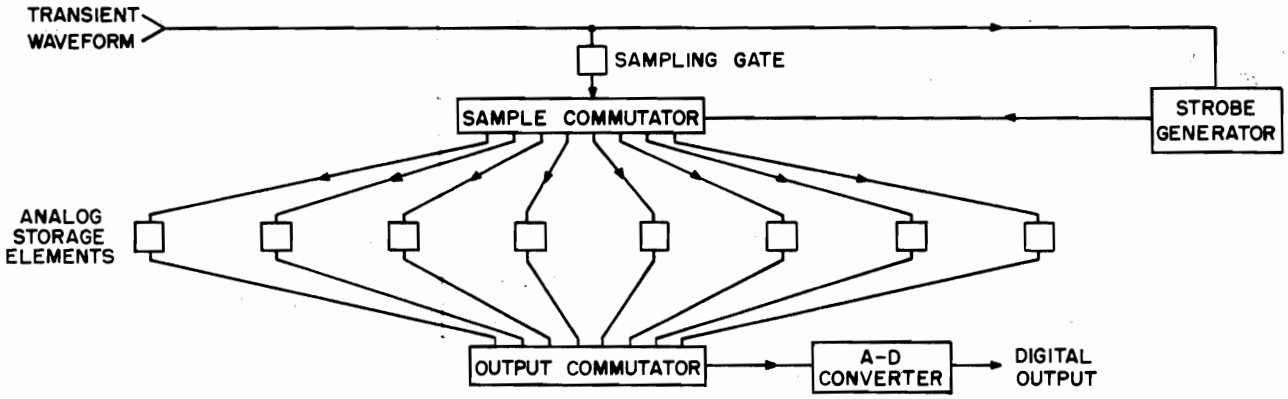


Fig. 6. Commutated fanout.

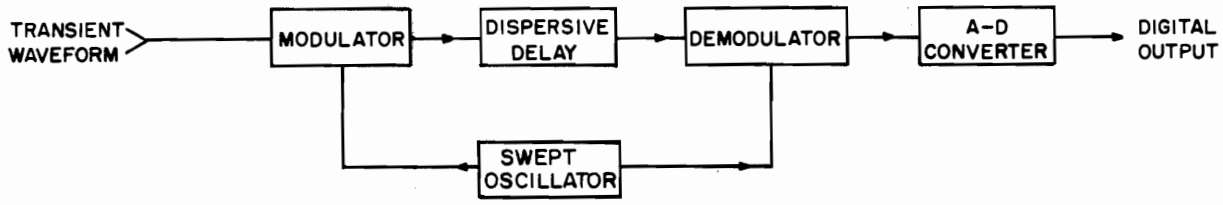


Fig. 7. Waveform stretcher.

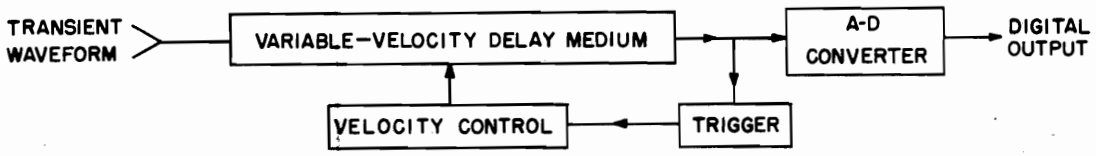


Fig. 8. Variable-velocity delay medium.

discussed in subsections A through G below. The block diagram and some examples relating to the second form are shown later in Figs. 9 through 12 and are discussed in subsections H through J.

A. The Scan Converter

Of the various techniques to be discussed, this device bears the closest resemblance to the conventional oscilloscope and camera combination. As in that approach, the first analog storage medium is a coaxial delay line which is followed by deflection circuitry which converts the signal amplitude and time into two orthogonal deflections. As is seen in Fig. 2, the phosphor screen of the oscilloscope is replaced by a pre-charged semiconducting target which retains the trace in the form of an enhanced positive charge pattern resulting from local secondary emission induced by an electron cascade initiated by the write beam. The data can remain in this form for a considerable length of time if so desired. Readout at a reduced rate is accomplished by use of a second, low energy, electron gun which scans the charged surface of the target. An electrical readout is obtained from a collector electrode whenever the sweeping read beam encounters a charge-enhancement area. The amplitude and time coordinates of a point on the trace are represented by the deflection voltages of the readout gun at the time the read beam encounters the trace. These voltages are then converted into digital format by a relatively slow analog-to-digital converter and transferred to a digital storage medium. The analog-to-digital converter can be eliminated by generating the readout deflection voltages as stairsteps corresponding to discrete numbers and then writing this digital information directly into memory upon receipt of the collector electrode trace-interception pulse.

B. Segmented Delay Medium

This approach, shown in Fig. 3, uses sampling gates placed along a delay medium at spacings equivalent to the time resolution required for sampling the waveform. The signal is thus stretched out in space over the length of the delay medium. When all of the sampling gates are strobed simultaneously, the magnitude of the signal at each point on the line is transferred to an associated analog storage element. The waveform samples thus stored decay gradually at a rate depending on the type of storage element, e.g., capacitors whose charge leaks off slowly. Before the waveform can deteriorate appreciably, an electronic or mechanical commutator successively interrogates the analog storage elements and transfers the stored values to an analog-to-digital converter. The successive digitized voltages are then stored in a digital memory.

Instruments using this approach have been envisioned using optical delay lines, and as long ago as 1962 a simple instrument using coaxial delay line intended for inclusion in a rocket payload was constructed at the Livermore Laboratory of the Lawrence Radiation Laboratory. More sophisticated versions have been built there since. Thus far such devices have been limited to a very small number of samples.

The primary difficulties to be overcome to make this approach practical are: (a) the dispersion and attenuation of the long delay medium, (b) the physical volume requirements of the medium, (c) the mismatches caused by the sampling gates coupled to the delay segments, and (d) the large number of gates and storage elements required.

In principle a simpler version could be constructed by using normally closed links in series with coaxial delay segments to break the segments into individual capacitors upon receipt of simultaneous strobe pulses. The difficulty here is in constructing links which do not mismatch the line while closed and which furnish a sufficiently high impedance when opened electronically.

C. Recirculating Delay Medium

This technique utilizes a re-entrant delay medium whose length is greater than the length of the waveform to be sampled. Entrance to the delay is controlled by a steering gate as shown in Fig. 4. The signal continuously circulates around this medium and is sampled by the single sampling gate once per pass. The sampling gate is strobed slightly later on each pass of the signal, and hence its successive outputs represent successive points along the waveform. Each of the samples is stored temporarily in an analog storage element which is interrogated between passes and the sample converted

to digital form. Samples are thus obtained at an equivalent sampling rate whose period is the difference between the true sampling period and the time required for one pass of the signal around the loop.

An optical delay line version of this approach is being attempted at the Santa Barbara division of EG&G, Inc.

The obvious disadvantage of this technique is that the signal must traverse the entire delay medium as many times as samples are desired, and hence the attenuation and dispersion thus far have ruled out this possibility. Possible approaches to improved delay media will be discussed in a later section. Even if these succeed, there is still the problem of building a switch or gate to make the delay medium re-entrant.

D. Fanout

Here the signal is presented simultaneously to a large number of identical sampling gates, as illustrated in Fig. 5. These gates are all closed until a trigger signal is received. At this time the gates are strobed successively, with the time from the strobe of one gate to the strobe of the next being the time resolution desired, and the total time span being the product of the interstrobe time and the number of sampling gates. Since only one gate is open at a time, the input impedance of the gates is designed to be very high in the closed condition, and equal to the terminating impedance for the input cable during the gate-open period. The sampling gates transfer the signal samples to an associated bank of analog storage elements which retain the signal distributed in space in analog voltage form. A commutator subsequently interrogates these elements and transfers the successive voltage samples to an analog-to-digital converter and thence to digital storage. Note the similarity to the Segmented Delay Line approach--in one case the signal is distributed in space by a delay medium, while in the other case the strobe is distributed.

This technique is promising, and has been used in a number of preliminary attempts. One problem, which is common with the segmented delay medium, is the large number of gates and storage elements required. Possible approaches to solving this difficulty will be discussed in a later section.

E. Commutated Fanout

Instead of the bank of sampling gates used in the previous approach, Fig. 6 illustrates a technique wherein a single gate and a commutator are used to divert successive samples to a bank of analog storage elements. The remainder of the system is identical to that of the previous illustration.

F. Waveform Stretcher

This technique uses frequency conversion and dispersion to stretch out the signal in time. We see in Fig. 7 that the signal first modulates a local oscillator signal whose frequency is swept during the course of the transient. The modulated swept-frequency carrier then passes through a delay medium of controlled dispersion whose envelope delay is proportional to frequency. Since the envelope of the modulated signal is the input waveform, the later portions of this waveform are thus delayed in time. A demodulator extracts the stretched-out waveform from the carrier, and this waveform is then amplitude digitized and stored.

A feasibility demonstration model has been built by an aerospace company, but is a long way from being usable at this time. Obtaining a sufficently well controlled large dispersion ratio and making mixers work uniformly and efficiently over the frequency range present tremendous difficulties. The dispersive delays are still rather bulky.

G. Variable-Velocity Delay Medium

In the approach outlined in Fig. 8, the signal propagates into a delay medium whose velocity of propagation may be altered electrically. Before the leading edge of the waveform reaches the far end of the medium, its velocity is decreased either abruptly or gradually. The signal exits at low velocity, which stretches it out in time, and may be digitized by a relatively slow amplitude converter. The delay medium could, for example, take the form of a transmission line whose equivalent series inductance per unit length L and capacitance per unit length C are electrically alterable. They could be increased in the same ratio so that

the characteristic impedance $\sqrt{L/C}$ remained constant while the characteristic velocity $\sqrt{1/LC}$ decreased.

The variable-velocity technique has been used in the case of a microwave carrier propagating as a magnetoelastic wave or spin wave in an yttrium-iron-garnet (YIG) crystal. The velocity of propagation is controlled by a magnetic field applied to the crystal. The carrier is modulated by the transient waveform, and hence this approach bears a superficial resemblance to the stretch approach described earlier. The proposal of this section, however, is to operate directly on the signal waveform rather than on a modulated carrier. One promising approach has been developed by the Elcon Laboratory, which has constructed an ion-beam delay line which carries the signal as a beam-intensity variation. Delay is achieved by the travel time of the ion beam through an equipotential drift space filled with plasma. Magnetic and/or electrostatic sheath focussing are used to control the particle trajectories. The relatively low velocity of the massive ions may be controlled by the applied accelerating potential. A bandwidth of 40 MHz has been achieved and this does not appear to be a limitation. Voltage-controlled delays from microseconds to milliseconds appear to be feasible.

Figure 9 is a block diagram of the approach considered in the next three subsections, wherein analog-to-digital conversion of the signal voltage precedes time conversion.

H. Electron-Beam Converter Tube

This is an early example of an approach to real-time analog-to-digital conversion. The first such tube was originally developed at the Bell Telephone Laboratories back in 1947. A tube capable of a 10-MHz word rate with a resolution of five bits had been developed by 1951. In this device, the signal voltage is used to deflect an electron beam in much the same manner as in an oscilloscope tube or scan converter. The deflected beam passes through an aperture mask which contains a digital pattern of openings, and impinges upon a series of collector electrodes. The current pulses from these electrodes form a digital representation of the beam deflection. This tube was intended for continuous digitizing of television signals, rather than for waveform storage in digital form. A higher-frequency version could be constructed and used in the configuration illustrated in Fig. 10, where a commutator directs the parallel digital words to a succession of word storage locations in memory, with the commutator performing the function of conversion from time separation of data points to a spatial separation.

I. Light-Beam Deflection Conversion

This scheme is closely related to the electron-beam deflection technique. A laser beam is deflected by an electro-optical director and passes through an aperture plate to a bank of photoelectric detectors as sketched in Fig. 11. The current pulse outputs of these detectors are processed in the same manner as are the outputs of the electron-beam deflection tube. Light deflectors which could possibly be used for this purpose have been developed for optical modulators and computers, and for optical recording on film. However, at the present time these still have limited frequency response and sensitivity.

J. Solid-State Converter

The two beam-deflection techniques described above offer few advantages over the oscilloscope or scan converter. In the solid-state converter of Fig. 12 we have direct analog-to-digital conversion without use of a vacuum envelope or of a laser. This approach has the advantages of simplicity, reliability, compactness, and low power consumption. The signal is sampled at a rate appreciably greater than twice the highest frequency of interest (sampling-rate considerations are discussed in Section VIII), and the samples are compared to digital reference voltages in high-speed comparators. The comparator outputs are converted to a parallel digital format and a commutator or shift register performs the subsequent time conversion. If sufficiently fast electronic circuitry can be developed, this approach promises to be the most practical of all those described. Numerous techniques for fast analog-to-digital conversion are discussed in Section IV. The particular diagram shown in Fig. 12 illustrates an approach which is a compromise between simplicity, directness, and speed of response.

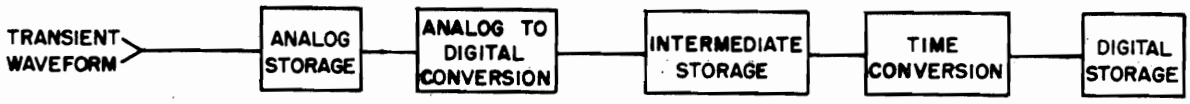


Fig. 9. Block diagram—amplitude conversion preceding time conversion.

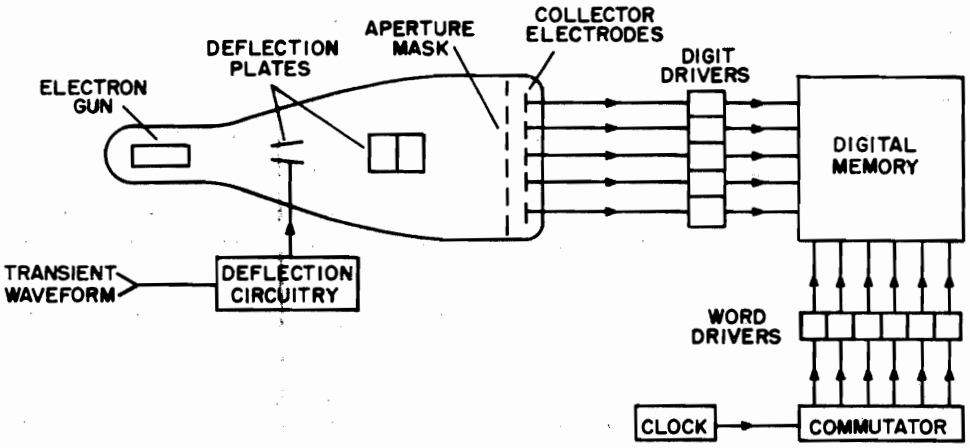


Fig. 10. Electron-beam converter tube.

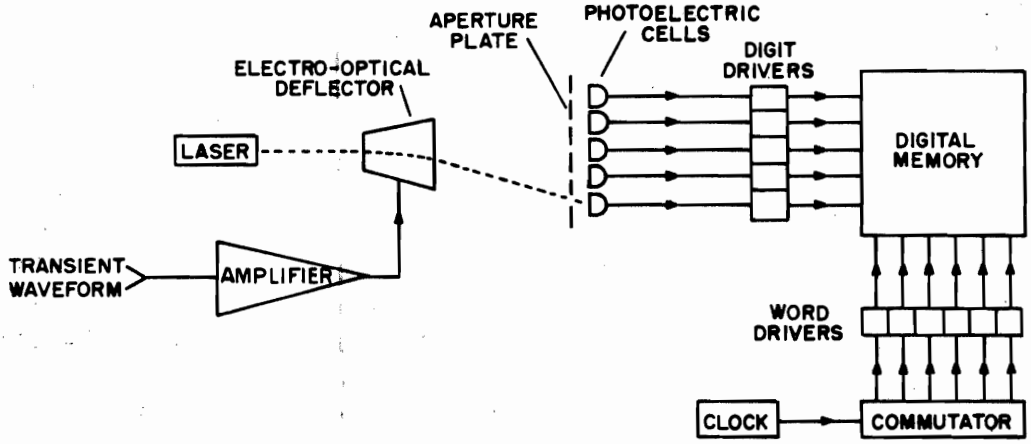


Fig. 11. Light beam deflection conversion.

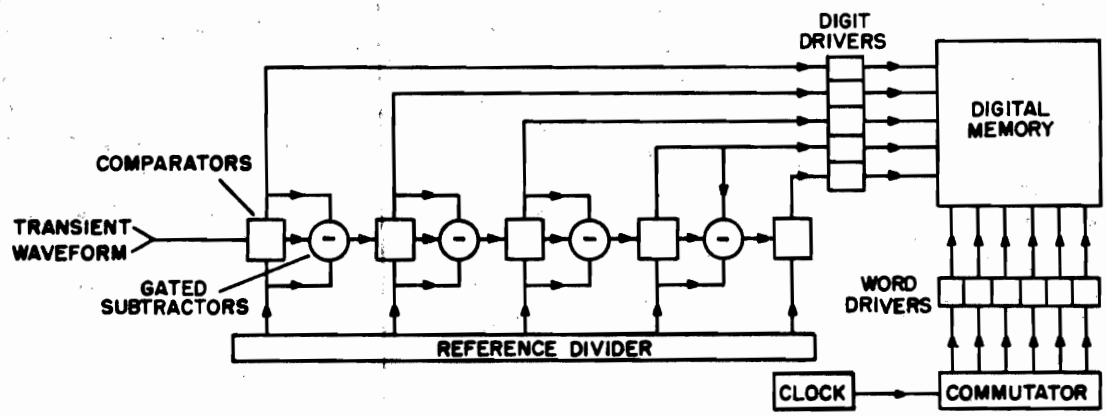


Fig. 12. Solid-state converter.

IV. RECORDING SYSTEM CONSTITUENTS

There are a number of basic recording system elements which are common to several of the approaches outlined in the previous section. In the following paragraphs we shall discuss some of the methods by which these constituents may be realized and compare their relative advantages and disadvantages.

A. Sampling Gates

Sampling gates are used to transfer a short sample of the signal from one analog storage medium to another upon receipt of a sampling control pulse or strobe pulse. The ideal sampler must transfer a repeatable fraction of the signal present at its input each time it is strobed, and must not introduce any pedestal or feedthrough of the strobe pulse. The former objective may be achieved by making the impedance of the forward conducting path of the gate very small compared to the impedances of the source and the load. One attempts to realize the second objective either by making the gate inherently balanced or by deliberately introducing cancelling strobe feedthrough signals.

By far the commonest form of sampling gate is the diode bridge illustrated in Fig. 13. In the absence of a strobe pulse the diodes are back-biased and form a high-impedance path between the source and the load. The strobe pulse biases the diodes into conduction and effectively couples the source to the load for the duration of the strobe. In the resistive drive approach of Fig. 13a, isolation of the signal and strobe is accomplished by the relatively high resistors in the strobe current path. In the transformer-driven bridge, Fig. 13b, this isolation is achieved by the common mode rejection of the transformer. A transistor-driven version of Fig. 13a is sometimes used, in which the resistors are replaced by the collector resistances of a pair of complementary driving transistors. Capacitive feedthrough of the strobe pulse may be minimized in all three cases by use of small trimming capacitors. The sampled signal will always be the same fraction of the input signal magnitude if either the sampling strobe pulse is always of constant width and magnitude, or if the source and load impedances are of the same type, i.e., both resistive or both capacitive or inductive, and the series impedance of the bridge is negligible during conduction.

The transformer-coupled half bridge illustrated in Fig. 14 uses transformer input coupling to minimize the problems of capacitive feedthrough of very fast rise strobe pulses, and has only half the series resistance of the bridge type. These improvements are somewhat offset by the aberrations introduced by a less than perfect transformer. The two secondary windings must be well balanced both magnetically and capacitively. Numerous versions of this circuit with slightly different winding configurations are possible.

In order to pass short samples with high efficiency and to present a high impedance in the gate-closed condition, the diodes used in the bridges described above must be high-conduction types with low voltage drop, a minimum of charge storage, and a high ratio of back to forward resistance. Where signal voltages are high, hot-carrier diodes are used for their lack of minority-carrier storage. Where signal voltages are low, back diodes (tunnel rectifiers) are sometimes used for their low forward voltage drop.

In some cases controlled active-element coupling may afford some advantages over the use of passive diodes. In Fig. 15a, field-effect transistors are used as the coupling elements. These devices can have very large ratios of on-to-off resistance. Complementary devices are used and are driven with bipolar strobe pulses in order to effect a cancellation of the capacitive feedthrough terms. The transistor bridge of Fig. 15b operates in the same manner as the basic diode bridge of Fig. 13a, but the loading of the source and the impedance seen by the load are lowered through the use of the active devices.

The magnetic modulator gate of Fig. 16a has been used when the signal was available as a current on a transmission line and a measure of this current was to be transferred to an analog magnetic storage device. Instead of coupling the signal directly to the receiving storage element, the signal is used to modify the inductance of a core. A strobe pulse passed through this core and through the secondary magnetic element has its magnitude modulated by the varying inductance of the core, and hence the perturbation of the strobe pulse

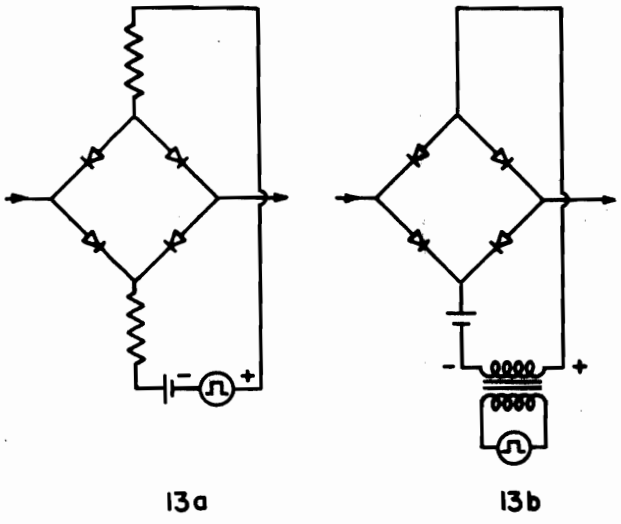


Fig. 13. Diode bridge gate.

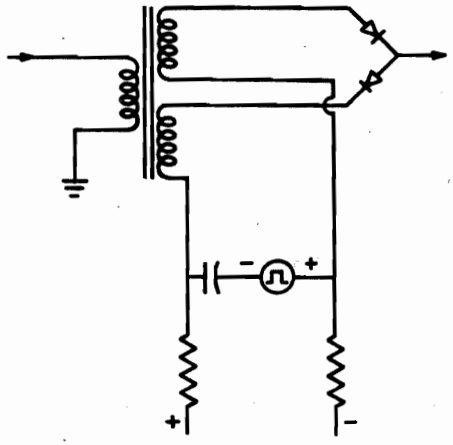


Fig. 14. Transformer-coupled half bridge.

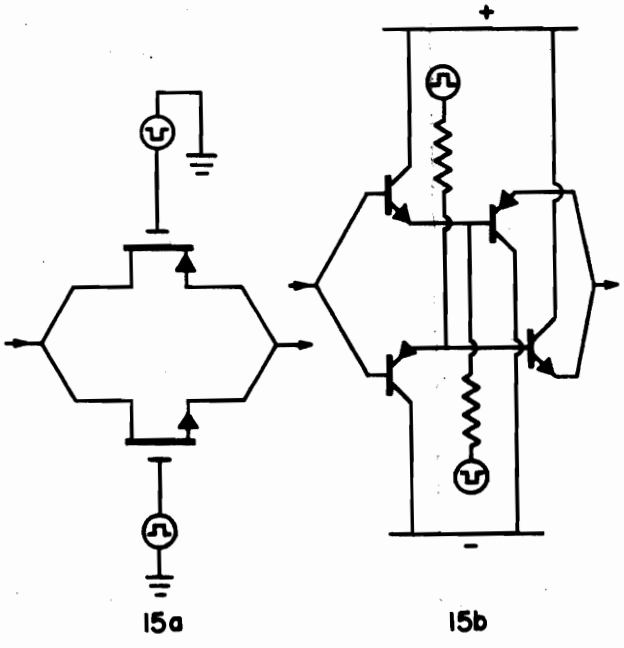


Fig. 15. Active element coupling.

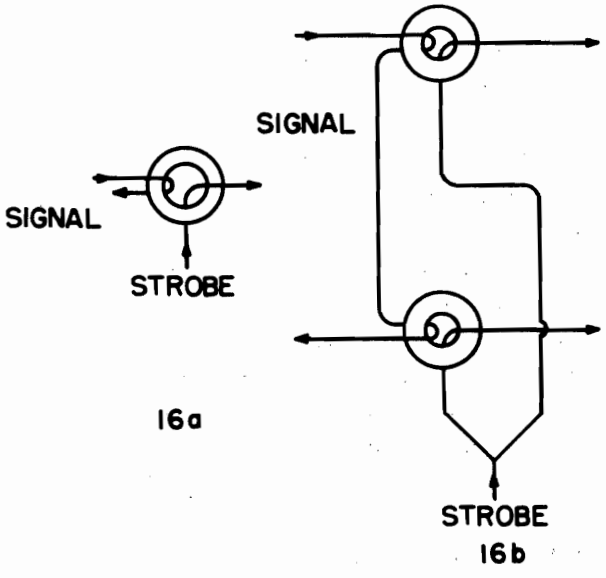


Fig. 16. Magnetic modulator.

seen by the storage element is a measure of the signal current. Since this approach is inherently nonlinear, a bipolar or push-pull arrangement is used as in Fig. 16b, in which the signal current modulates two cores and a pair of strobe pulses pass through these two cores and into two analog storage elements used in a differential mode.

B. Analog Storage Elements

Analog storage elements are required in systems where the time axis conversion precedes amplitude conversion. The choice of storage element is determined by considerations of impedance level, the amount of time available for storing the information, and the length of time for which the information must be held. The simplest and commonest forms of analog storage are charge storage on a capacitor and magnetic energy storage in an inductor.

An approach which is not quite so obvious is analog magnetic storage in ferrite cores. Ordinarily these devices are thought of as only being suitable for binary storage. The hysteresis loop of a typical ferrite core is sketched in Fig. 17. Assume that the core is initially in the state represented by point A. A slowly increasing magnetic field or winding current will cause the state of the core to move along the solid line path A→C→D. Removal of the current now could permit the core state to relax along the dotted line path D→E. The remnant flux at point E is directly related to the maximum winding current at point D. Thus, it is possible to have analog magnetic storage, albeit there is a nonlinear relationship between the stored flux and the applied current.

If a magnetic field of magnitude less than the distance a→c is applied and removed, essentially no change of magnetic state takes place. Let a signal current whose peak value is less than a→c be passed through a signal winding on the core. No storage will take place. Now add a relatively slow strobe current pulse of magnitude c→d in a strobe winding. The core will move to state D. Upon termination of the strobe current the core will fall to the point C′. At the end of the signal pulse the core state will go to E. The result is that the signal can be strobed into the core and that the relationship between the stored flux and the signal at strobe time has been linearized.

The time required to traverse the path A→C→D is determined by the propagation time within the ferrite material. If the current pulse had had a very short rise time the state of the core would follow the dotted path A→C→F, indicating that at each level of current the flux change was lagging behind. Upon cessation of the current the core state would follow path F→G, with the core retaining the flux represented by point G. Thus, it is possible to obtain analog magnetic storage for fast current pulses, but the pulse magnitudes required are greater and/or the resulting flux change is smaller.

Readout may be accomplished by interrogating the core with a read pulse and determining the amount of flux switched (by integrating the voltage pulse induced in a sense winding). Such readout is, of course, destructive. Nondestructive readout may be obtained by incorporating the core in an oscillator circuit whose frequency is determined by the amount of unsaturated core, or by using a multiaperture core, commonly called a Transfluxor, as illustrated in Fig. 18. The analog storage is accomplished in the main aperture with the partial switching of the flux around this aperture being the measure of the applied current pulse. Readout is accomplished by passing a read pulse through the auxiliary aperture, which permits generating a flux reversal signal in the sense winding without destroying the flux state around the main aperture.

Faster storage may be obtained by using thin magnetic films, since in such films switching is accomplished by domain-wall rotation, which is orders of magnitude faster than bulk magnetization. These devices are constructed by vacuum deposition of a magnetic alloy such as Permalloy upon a suitable mechanical substrate such as glass. To achieve the magnetic properties desired for a storage element, a magnetic field is applied parallel to the plane of the film during the deposition process. The result is that the magnetization of the film tends to remain permanently aligned in this direction. When the film is subsequently used as a storage element, a magnetic field applied in the same plane but transverse to the direction of the remnant magnetization will tend to rotate the magneti-

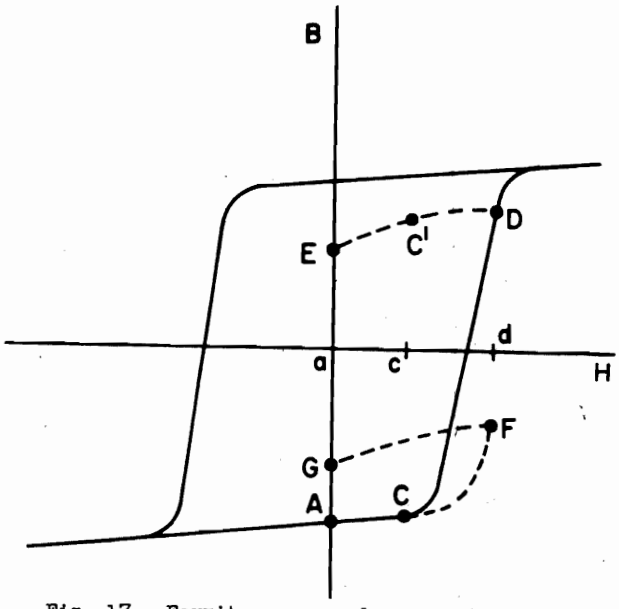


Fig. 17. Ferrite core analog magnetic storage.

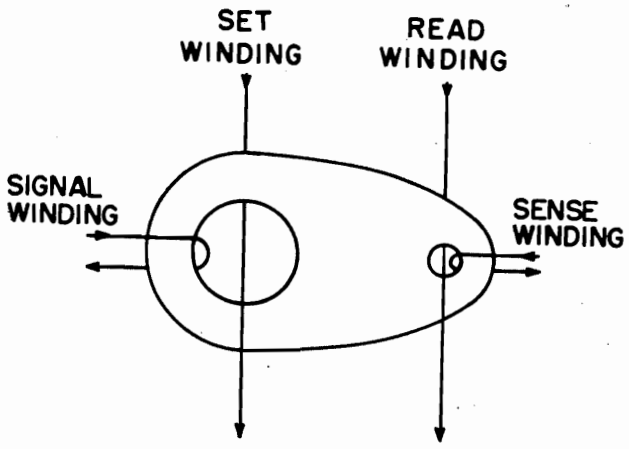


Fig. 18. Transfluxor.

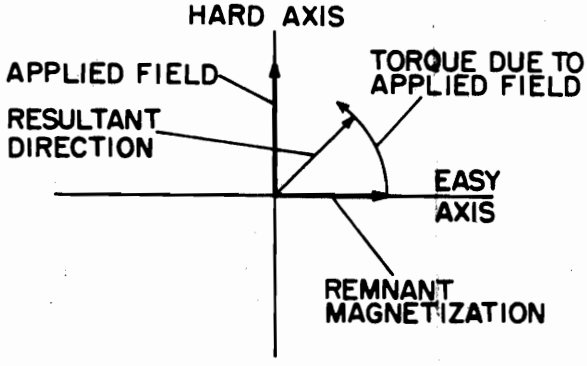


Fig. 19. Transverse field applied to thin magnetic film.

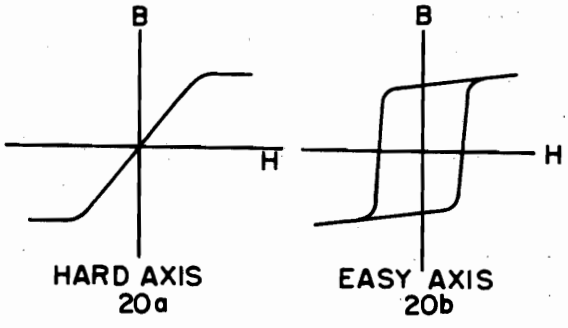


Fig. 20. Thin magnetic film hysteresis loops.

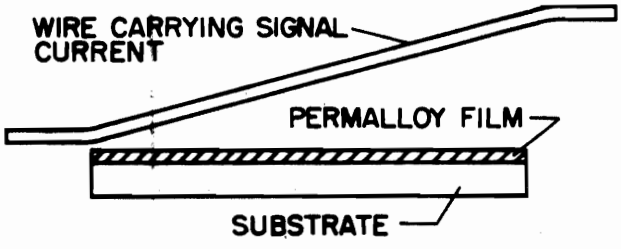


Fig. 21. Storage by partial area switching of thin magnetic film.

zation as sketched in Fig. 19. When all the domains have rotated 90 degrees, the film is saturated. Upon removal of the torque due to the transverse field, the film magnetization tends to return to the original direction, with the resulting hysteresis loop for the transverse, or hard, direction appearing as in Fig. 20a. A field applied opposing the natural magnetization axis, or easy axis, at first exerts no torque on the remnant magnetization. As this field is increased, eventually all the domains tend to rotate together suddenly to align with the applied field, with the resulting hysteresis loop for the easy axis being of the form shown in Fig. 20b. This domain-wall rotation can take place in times less than a nanosecond, so one now has available a very high speed magnetic storage element. This device may be used either for binary storage or for analog storage, using the same technique as described above for the ferrite core. Fields in the appropriate directions are normally applied by means of conductors laid across the surface for the film, but one recent development uses wires passed through holes in the substrate.

A different approach to thin film analog storage was used in a device constructed by personnel of the Sandia Laboratory. This device uses complete switching of the film with the physical extent of the switched area being an approximately linear measure of the applied current. The film is seen edge-on in Fig. 21, with the signal wire placed at an angle above it. The field at the surface of the film is strongest at the left edge and becomes progressively weaker as the spacing between the wire and the film increases. The film is switched below the wire at the left edge, and the switched area extends as far to the right as is permitted by the condition that the field due to the signal current exceeds the critical field required for switching of the film.

Ferroelectric devices are just now beginning to show promise as storage elements. These devices have electrical hysteresis loops of the same general form as the more familiar magnetic hysteresis loop, and hence may be applied in an analogous manner. Whereas magnetic elements are current-operated devices, the ferroelectrics are voltage-operated devices, and so far have tended to be high-impedance, and hence slower, devices.

The capacitive and inductive storage elements mentioned at the beginning of this section represent volatile storage and the analog data stored in them must be further processed without delay. The ferromagnetic and ferroelectric devices, on the other hand, can store the information for long periods of time. This makes possible a physical separation of the storage and readout functions in a manner analogous to the separation of recording on film and the subsequent film development and reading in the conventional oscilloscope-camera combination.

C. Delay Media

Suitable delay media for recording techniques such as the segmented delay medium and the recirculating delay medium approaches are virtually nonexistent. The only possible choices appear to be conventional coaxial cables, cryogenic or superconducting cables, and optical delay lines. Other delay media such as microwave waveguides, and acoustic wave propagation in glass, quartz, and wire have been used for digital storage, but the very high dispersion of these media renders them unsuitable for analog waveforms at this time. Even conventional coaxial cables, which ordinarily are considered to be good delay media, are limited to relatively short delays when faithful storage and reproduction of a waveform are required. This comes about because the high-frequency attenuation and excess phase delay caused by skin effect losses tend to make the risetimes of such cables proportional to the square of the delay time. The impulse-function response and the step-function response of a skin-effect-limited coaxial cable (coax) are indicated respectively in Eqs. 1 and 2:

$$g(t) = \sqrt{\frac{\tau}{\pi}}\, t^{-\frac{3}{2}} \cdot \exp\left(-\frac{\tau}{t}\right) \qquad (1)$$

$$h(t) = 1 - \operatorname{erf}\sqrt{\frac{\tau}{t}} = \operatorname{erfc}\sqrt{\frac{\tau}{t}} \qquad (2)$$

where

$$\tau = \left(\frac{kz}{2}\right)^2 \qquad (3a)$$

$$k = \sqrt{\frac{\varepsilon}{\sigma}} \cdot \frac{1 + \exp(x)}{2 R x} \qquad (3b)$$

$$x = \ln\frac{R}{r} = \frac{2\pi\sqrt{\varepsilon_r}\, Z_o}{\eta} = \frac{\sqrt{\varepsilon_r}\, Z_o}{60} \qquad (3c)$$

and where z is the length of the delay line, ϵ is the permittivity of the dielectric, σ is the conductivity of the conductor material, R is the inner radius of the outer conductor, r is the radius of the center conductor, ϵ_r is the relative permittivity of the dielectric material, Z_o is the characteristic impedance of the cable, and η is the intrinsic impedance of space in MKS units.

The complementary error function step-function response of Eq. 2 has an initial rapid rise followed by a very slow approach to the final value. The result of this is that the time required for the step response to rise from 10% to 90% of the final value is very long in units of the time constant τ:

$$\text{10\%-90\% risetime} \qquad \Delta t = 126.1\,\tau \tag{4}$$

This very slow approach to the final value is the factor which makes conventional coax delay lines unsuitable for long delays. We see from Eqs. 4 and 3a that the risetime is proportional to the square of the cable length and hence to the square of the delay time. A more useful form may be found by using the approach outlined below.

The frequency response of a cable is the Fourier transform of the impulse response of Eq. 1:

$$H(\omega) = \exp\left[i(\omega t - kz\sqrt{\tfrac{\epsilon}{2}})\right] \cdot \exp\left(-kz\sqrt{\tfrac{\epsilon}{2}}\right) \tag{5}$$

The attenuation in decibels is then

$$a = -20 \cdot \log_{10}|H| = -20 \cdot \log_{10} e \cdot \ln|H|$$
$$= 20 \cdot \log_{10} e \cdot kz\sqrt{\tfrac{\epsilon}{2}} \tag{6}$$

Combining this with Eq. 3, we obtain an expression for the time constant in terms of the attenuation at a given frequency. In Eq. 7, the time constant τ is expressed in nanoseconds, the total attenuation a is in decibels, and the frequency is in MHz.

$$\tau = 1.055\,\frac{a^2}{f} \tag{7}$$

The attenuation in terms of the delay time is

$$a = Az = A\,v\,T = A\,\frac{c}{\sqrt{\epsilon_r}}\,T \tag{8}$$

where A is the attenuation per unit length and T is the delay time.

Substituting,

$$\tau = 1.055\,\frac{A^2 c^2 T^2}{f\epsilon_r} \tag{9}$$

The 10%-90% risetime is then

$$\Delta t = 133.0\,\frac{A^2 c^2 T^2}{f\epsilon_r} \tag{10}$$

The delay-to-risetime ratio, which is a measure of the fidelity with which a transient of a given length may be stored, is then

$$\frac{T}{\Delta t} = \frac{f\,\epsilon_r}{133\,A^2 c^2 T} = 77.7\,\frac{f\,\epsilon_r}{A^2 T} \tag{11}$$

where the attenuation A is here expressed in the commonly tabulated units of db/100 ft at the frequency f in MHz, and the delay T is in nanoseconds.

If we insert into Eq. 11 the characteristics of a typical coaxial cable such as RG-8A, we obtain $T/\Delta t = 4468/T$, which indicates that for a delay of, say, 1000 ns, this cable would be hopelessly poor as a storage medium. Smaller cables, which would be more appropriate for obtaining a reasonable amount of delay in a small package, are considerably worse.

This situation may be alleviated considerably by operating delay lines at cryogenic temperatures. The residual resistivity of copper at very low temperatures is between 1% and 0.2% of that at room temperature, depending on the purity of the copper. We note from Eq. 3 that the factor k is proportional to the square root of the resistivity and hence that τ is directly proportional to the resistivity. In some cases this may be a sufficient improvement to make the use of conventional coaxial cable possible.

The obvious next step is to go to superconducting coax. Such cables have been constructed by a number of investigators, with the commonest construction being a niobium center conductor, teflon dielectric, and a lead outer conductor. Niobium becomes a superconductor below 8.7°K, and lead does so below 7.2°K. Results with these cables have been spectacularly successful, with the rise time being limited only by the nonsuperconducting portions of the system. The major difficulties with this approach are in the need for a cryogenic environment and in the difficulty of fabricating long uniform pieces of cable. The best cables constructed have used a vacuum-deposited lead outer conductor, but this approach does not seem to be feasible for inexpensive large-scale production. A less expensive approach is to use an extruded or pressure-welded lead outer jacket, but this approach has the difficulty that it is almost impossible to obtain a uniform characteristic impedance. The latter problem has frustrated attempts to use superconducting lines as recirculating delay media. The segmented delay line recording technique suffers from the requirement that the sampling gates spaced along the delay line segments must be in the cryogenic medium if the delay line is not to have numerous points of exit from the low-temperature region.

Optical delay lines have also been considered, since a light beam undergoes little dispersion over an air path of the length required for a time delay of the order of a microsecond. It is not, of course, possible to propagate light through solids or liquids for this length of time without undue attenuation. Light beams have been used as storage media by reflecting the rays back and forth numerous times between pairs of curved mirrors. As many as 1000 reflections have been obtained with only a factor of four light loss. The primary source of light loss is scattering at the surfaces of the mirrors. This technique essentially amounts to delay of a high-frequency carrier modulated by the transient waveform. It suffers from the problems associated with all such modulation schemes, in that the modulation process may be nonlinear and/or require a large amount of modulating power. Modulators for light beams are particularly susceptible in the latter regard. In principle, one should be able to modulate a microwave beam and use this same technique, reflecting the beam between microwave mirrors. The volume requirements would seem to be formidable for either the optical or the microwave approach, since the velocity of progagation is of the order of one foot per nanosecond, and even one microsecond of delay would thus require 500 two-way passes between reflectors one foot apart. There also are stringent requirements upon the mechanical stability of such a resonator.

D. Analog-to-Digital Converters.

The ubiquitous analog-to-digital converter (ADC) is found in some form in every waveform recording system. In the case of the conventional oscilloscope-camera combination this may take the form of a film reader shaft angle encoder or a micrometer dial read by a human operator, but in all the recording systems considered here the ADC would be some form of electronic circuitry. In those few cases where the data is intended primarily for study by human beings, the converter output would be in decimal form, but the vast majority of data is intended for direct computer input and hence will be in the form of binary digits, or bits. Systems in which time conversion precedes amplitude conversion only require an ADC with modest speed capabilities, while those in which amplitude conversion takes place first require one which can work at the analog input data rate, and hence must have the full equivalent bandwidth. It should be noted here that the faster conventional ADC's on the market are considered here as only moderate speed devices. The forms of converters described below are listed roughly in order of increasing speed capability and/or accuracy.

The linear ramp ADC is shown in Fig. 22. In each sample period, a comparator is used to match the instantaneous value of the signal voltage with that of a linear voltage ramp which is restarted from zero for each sample. A counter begins registering clock pulses at the time the ramp starts. When the ramp voltage becomes equal to the signal voltage, the comparator stops the counter and the number appearing in the counter is then directly proportional to the signal voltage. The slope of the ramp is such that its voltage reaches full scale for the ADC in one sample period. The clock frequency is chosen so that the counter would indicate

the desired full scale number if permitted to count through the entire period. A divider on the clock output divides down the clock frequency so that a stop pulse is put out at the same time the counter would reach full scale for a full scale input signal. This divider output pulse resets the ramp to zero and resets the counter, and the converter is now ready to take the next sample. The content of the counter is read out immediately before reset and stored in a digital memory. The most obvious shortcomings of this approach are that its accuracy and resolution are determined by the repeatability and linearity of the ramp, and that there must be a dead period before reset of the counter in order to permit its contents to be read out. Another shortcoming is illustrated in Fig. 23a where the repeated ramp is shown superposed on the analog waveform. The points of intersection of the ramp with the signal are the points where the comparator stops the counter. It will be noted that the time spacings between these points are determined by the local slope of the input waveform, and hence that the sampling rate is not constant, and that the exact points in time at which the signal is sampled are not simply defined. However, it is possible to reconstruct these times in subsequent data reduction.

There are two relatively simple modifications which can improve the basic ramp ADC. The first is the use of a sample and hold circuit (S&H) which samples the input waveform at the start of each linear ramp and holds that value of the signal for the comparator throughout that sampling period, as illustrated in Fig. 23b. Although the ramp still reaches the sampled signal level at nonuniform points in time, the recorded voltage values are now known to correspond to the signal waveform at the beginning of each sampling interval. Operation of the ADC may be sped up by incorporating a self-resetting feature whose effect is shown in Fig. 23c. As soon as the comparator detects equivalence of the signal voltage and the ramp the counter is stopped, its contents are read out, and the cycle is repeated immediately. Once again the sampling intervals are nonuniform, but the average sampling rate has now been increased.

It is possible to make a major improvement in accuracy by noting that the numbers accumulating in the counter are equivalent to a very linear stair-step ramp. In the counter-type ADC illustrated in Fig. 24, the linear ramp is replaced by a stair-step voltage ramp generated by a digital-to-analog converter (DAC) which converts the counter reading to a proportional analog voltage. This is the basis of the majority of the less sophisticated converters on the market.

There are numerous forms of DAC's, but the basic principle on which almost all types operate is illustrated in Fig. 25. The binary output of the counter in parallel form is used to control semiconductor switches which gate weighted amounts of current to a current summing junction. This current is then converted to a proportional voltage, with the commonest technique being the use of an operational amplifier with a feedback resistor, as shown in the illustration. There are numerous alternative forms which the resistor network which generates the weighted currents may take, but their net effect is always as shown.

A great deal of time is wasted in resetting the counter to zero at the beginning of each sampling period and then waiting for the count to build up to the signal level. The continuous or up-down ADC in Fig. 26 overcomes this deficiency by use of a register which can either add or subtract counts. Once the converter is started, the comparator continuously compares the signal waveform to the output of the DAC and, depending upon whether the signal is higher or lower than the stair step, the counter is commanded to count up or down, respectively. The only break in continuous operation need be a periodic pause for reading out the contents of the counter.

Whenever the signal makes a sudden change, the continuous counter can only approach the new value at a rate determined by the size of the least significant bit and the clock frequency. A much more rapid approach to the new value could be obtained if the most significant bit were changed first and then less significant bits changed in decreasing order. This approach is used in the successive approximation ADC illustrated in Fig. 27. For each sample period the comparator first notes which of the signal or the output of the DAC is the larger, in order to determine the counting direction. The control logic then first tries a change of the

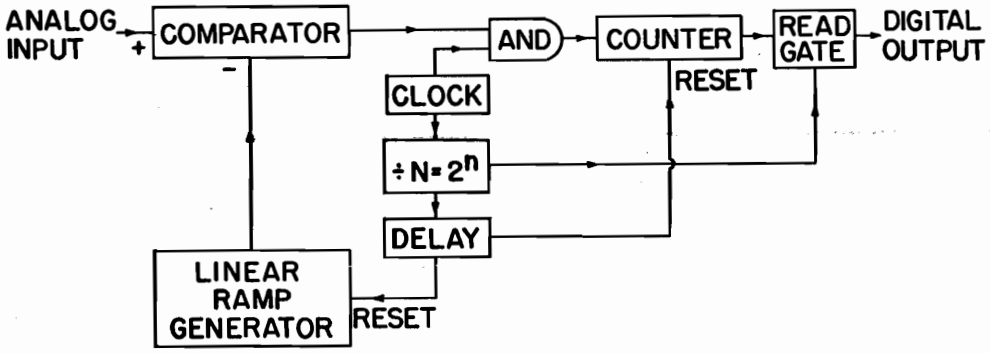


Fig. 22. Linear ramp ADC.

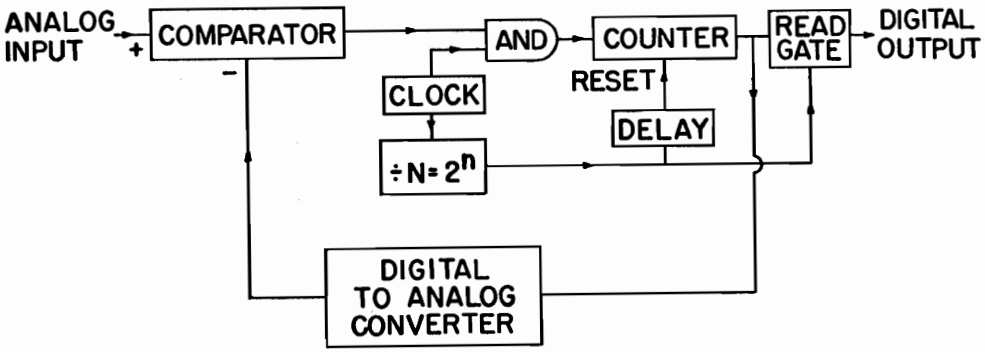


Fig. 24. Counter ADC.

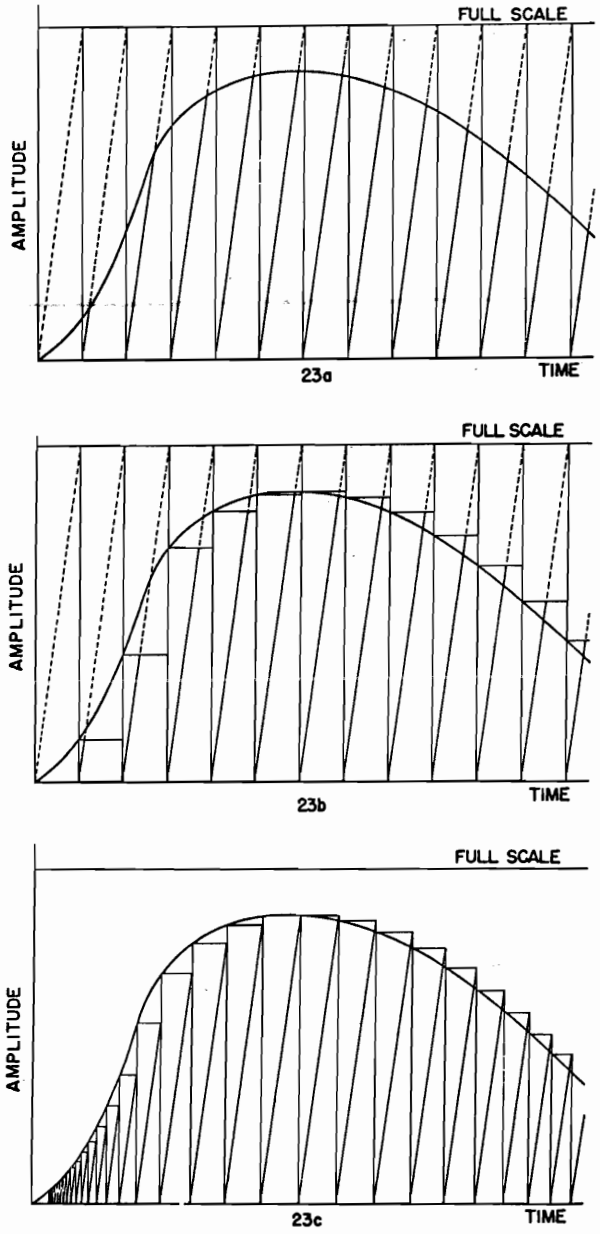


Fig. 23. Linear ramp sampling.

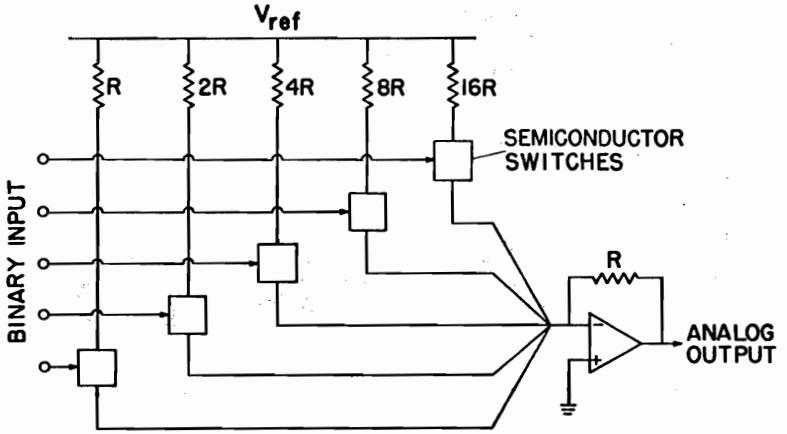


Fig. 25. Digital-to-analog converter.

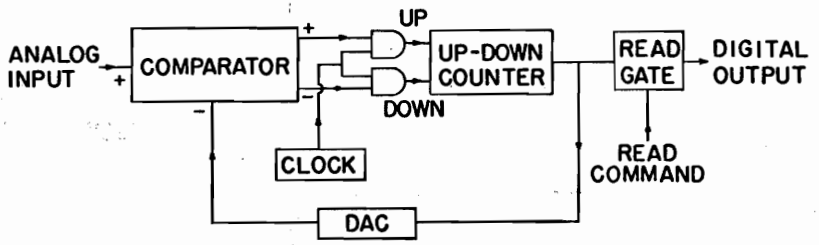


Fig. 26. Continuous or up-down ADC.

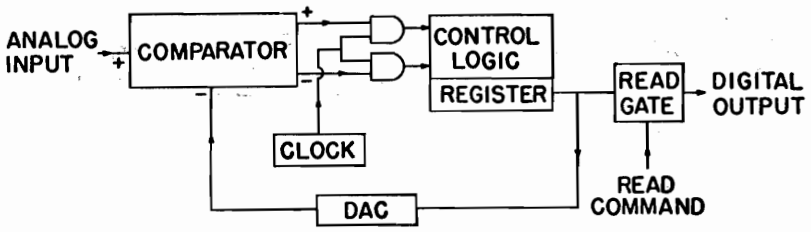


Fig. 27. Successive approximation ADC.

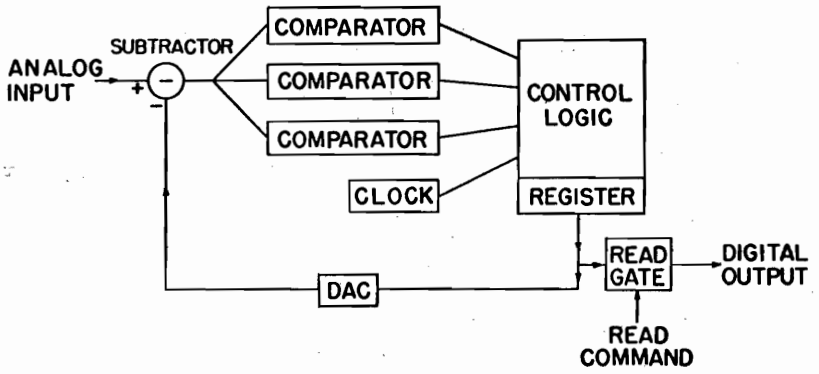


Fig. 28. Quantizing ADC.

most significant bit. The resulting new output of the DAC then indicates to the comparator whether or not this "first guess" was correct. If so, this bit is retained and the next less significant bit is similarly tested. If the first bit change represented too great a step, the most significant bit is reset and the next less significant bit is tested. This process is repeated until the least significant bit is satisfied. In the up-down counter ADC a full-scale step of signal input would require $N = 2^n$ steps to satisfy the comparator. The successive approximation approach only requires n steps for a similar input change.

The successive approximation ADC requires appreciably more control logic than does the continuous converter. Intermediate approaches have been taken as economic compromises. In these devices several of the low order bits are initially set to ones at the beginning of each sample interval. The more significant bits are then operated upon as in the up-down ADC, which can require a maximum of 2^m steps, where m is the number of higher order bits. When this initiallizing operation has been completed the ADC reverts to a conventional up-down converter and the lower order bits are determined.

The successive approximation ADC and its derivatives require S&H circuits, because a change in the input signal level between the time of selection of the higher order bits and that of the lower order bits could result in a completely erroneous count. Another possible approach which has been tried is to make the higher order bit decisions partially revokable and to incorporate along with the lower order bit decisions a capability to generate correction bits to change the higher bits to ensure consistent numbers.

The successive approximation ADC has the weakness that at the beginning of each sample cycle the highest order bit is tested first, regardless of whether or not a large signal input change has taken place to justify such a drastic test step. It would be desirable to perform an initial test to see how great a change has taken place since the last sample, and hence to be able to choose the appropriate order bit for testing first. This approach is used in the quantizing ADC of Fig. 28. The content of the output register (in analog form via the DAC) is first subtracted from the instantaneous value of the input signal. The difference is supplied to a bank of comparators (here shown as three, which can define four intervals or two bits for conversion), which in turn inform the control logic as to which bit should be tested first. The remainder of the sequence is identical to that of the successive approximation ADC. The number of comparators may vary anywhere from $N-1 = 2^n-1$ down to the three shown, with the degree of sophistication in selection of the proper bit for initial testing being traded off against the complexity of the use of more comparators and control logic. When the number of comparators exceeds a small number such as four or eight, it becomes more efficient to use a separate comparator for each binary step and to have each comparator control its own particular bit level in the register, as seen in Fig. 29.

The clocking, counting, digital-to-analog conversion, and feedback paths of the previous approaches are time consuming and tend to limit the speed at which such ADC's can operate. A faster device would result if all comparators operated in parallel and all bits were determined simultaneously without subsequent further comparison with the signal voltage. Alternatively, the same effective result would be obtained if the highest order bit were determined directly by comparison with the instantaneous signal voltage, and then lower order bits were determined by the results of the first comparison rather than by subsequent references to the signal input. This technique is incorporated in the, sequential binary ADC of Fig. 30. In the first comparator the signal voltage is compared to half of the full-scale voltage. If the signal is greater than half scale, a binary "one" is generated and the comparator opens a gate which permits exactly half of the full-scale voltage to be subtracted from the signal voltage. A slight delay is incorporated in the signal path to permit the comparator to complete its work before the subtraction takes place. If the signal voltage is less than half scale, no binary digit is generated and no subtraction takes place. The resultant signal (which now is guaranteed to be less than half scale) then progresses to the second comparator, where it is compared to one fourth of full scale. This process is repeated for as many stages as are

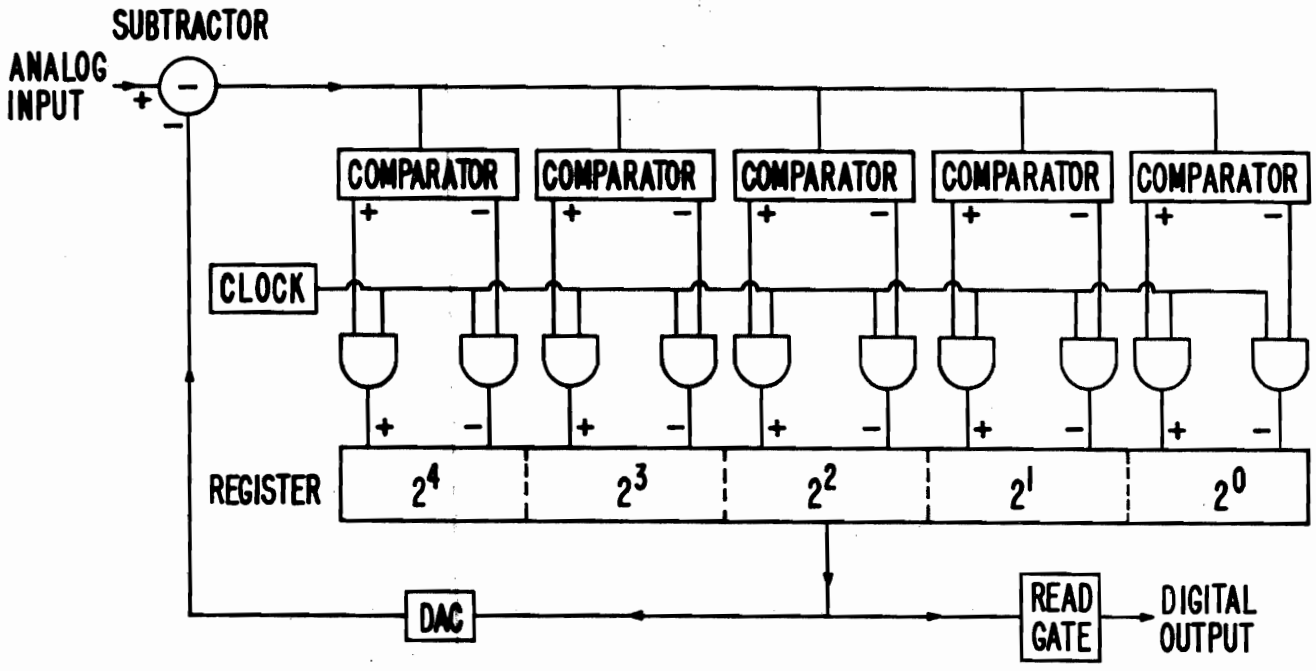


Fig. 29. Binary comparator quantizing ADC.

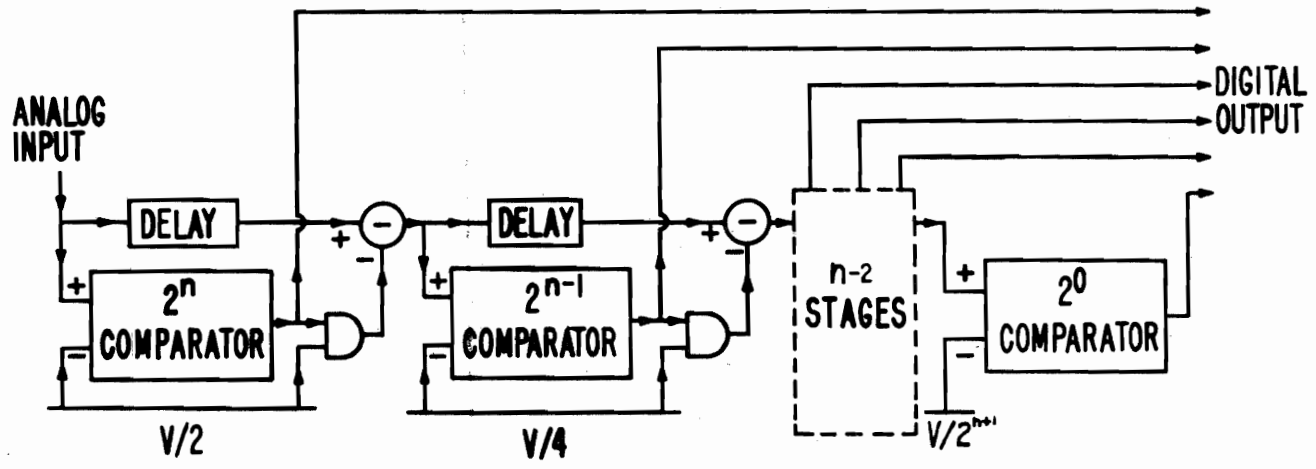


Fig. 30. Sequential binary ADC.

required to obtain the desired resolution. Once the (possibly modified) signal has left the first stage it is free to propagate independently through the remainder of the stages, and hence the first stage becomes available to operate on the next sample of the input waveform. We thus find that under steady-state conditions the first comparator is looking at the most significant bit of one sample of the input waveform while the second comparator is looking at the second bit of the previous sample, the third comparator is looking at the third bit of the second-previous sample, etc. The binary outputs of the comparators are in neither serial nor parallel form, but in a staggered array, with the higher order bits of the current samples being generated simultaneously with lower order bits of previous samples. A minor reordering of the binary data in digital storage is thus required subsequently. We note that by considering the successive comparator stages with their associated delays as a propagating system, we eliminate the need for an S&H circuit which would otherwise be required to prevent the signal from changing during the progress of conversion of a single sample.

The progressively decreasing reference voltages used as the signal progresses through the sequential binary ADC mean that the signal-to-noise ratio available to the comparators becomes progressively worse as the lowest order bits are reached. When bandwidth is not a severe problem, this decreasing-signal-level difficulty may be alleviated by inserting an amplifier with a precise gain of two at the output of each stage, immediately after the subtractor. If operational amplifiers are used, the subtraction can take place at the amplifier summing junctions. The net gain required (to have all comparators operate with a reference voltage of half of full scale) is equal to the reciprocal of the fractional resolution required, and hence the risetime of the signal residue at the last comparator will be degraded according to the expression $\Delta T = \sqrt{n(\Delta t)^2} = \sqrt{n} \cdot \Delta t$, where Δt is the risetime of one gain-of-two amplifier and ΔT is the overall risetime.

If a ramp function of signal which ultimately reaches full scale is applied to the signal input, the successive subtractions of the reference voltages each time the ramp reaches a new reference level will cause the resulting waveforms out of each of the first three subtractors of Fig. 30 to appear as in Fig. 31a, where we are considering an ADC without the additional x2 amplifiers. The sharp drops and corners on these waveforms and their progressive crowding together indicate that the bandwidth requirements of succeeding stages become increasingly severe.

Another difficulty with this type of converter is seen by reference to Fig. 32a, where the pattern of binary digits corresponding to the decimal numbers 0 through 15 is symbolized by shading. Note the line where a signal level of eleven units is represented by the binary number 1011. If the signal level were now to increase gradually to twelve units, three of the binary digits must change state simultaneously to arrive at 1100. Any lack of simultaneity in these state changes, particularly in the higher order bits, will result in an erroneous equivalent decimal number. The number of binary digits which must change simultaneously for each change of one unit of input is listed in the column to the right of the binary chart. This problem can be alleviated through the use of other codes than straight binary codes. There is a class of codes in which only one binary digit changes state for any transition from one signal level to the next. These codes are known as unit-distance codes, because on a multidimensional map containing all possible combinations of the specified number of digits, only one step is required to get from the point on the map representing one input signal level to the point representing the next higher or lower level. As an example, consider the unit cube sketched in Fig. 33, which represents the possible combinations of three bits. The first bit is plotted along the x axis, the second along the y axis, and the third along the z axis. Let a given signal level be represented by the binary number at any one of the corners of the cube. Then a unit-distance code is one such that the next resolvable higher or lower signal level is found at one of the three corners which may be reached by moving just one unit along one of the three cube edges which intersect at the chosen point. Numbers of more than three binary digits may be plotted on the corners of a hypercube, i.e., a cube of more than three dimensions. The

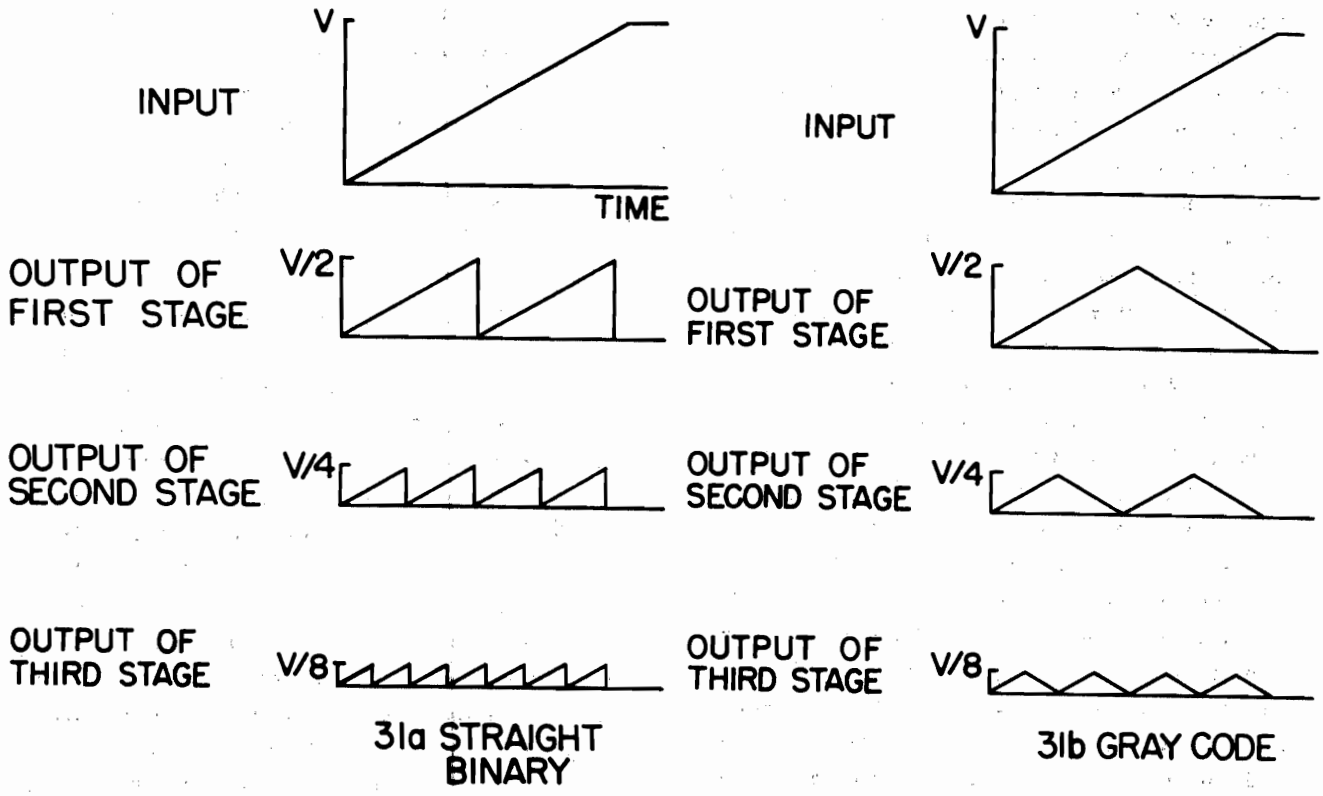


Fig. 31. Ramp waveforms.

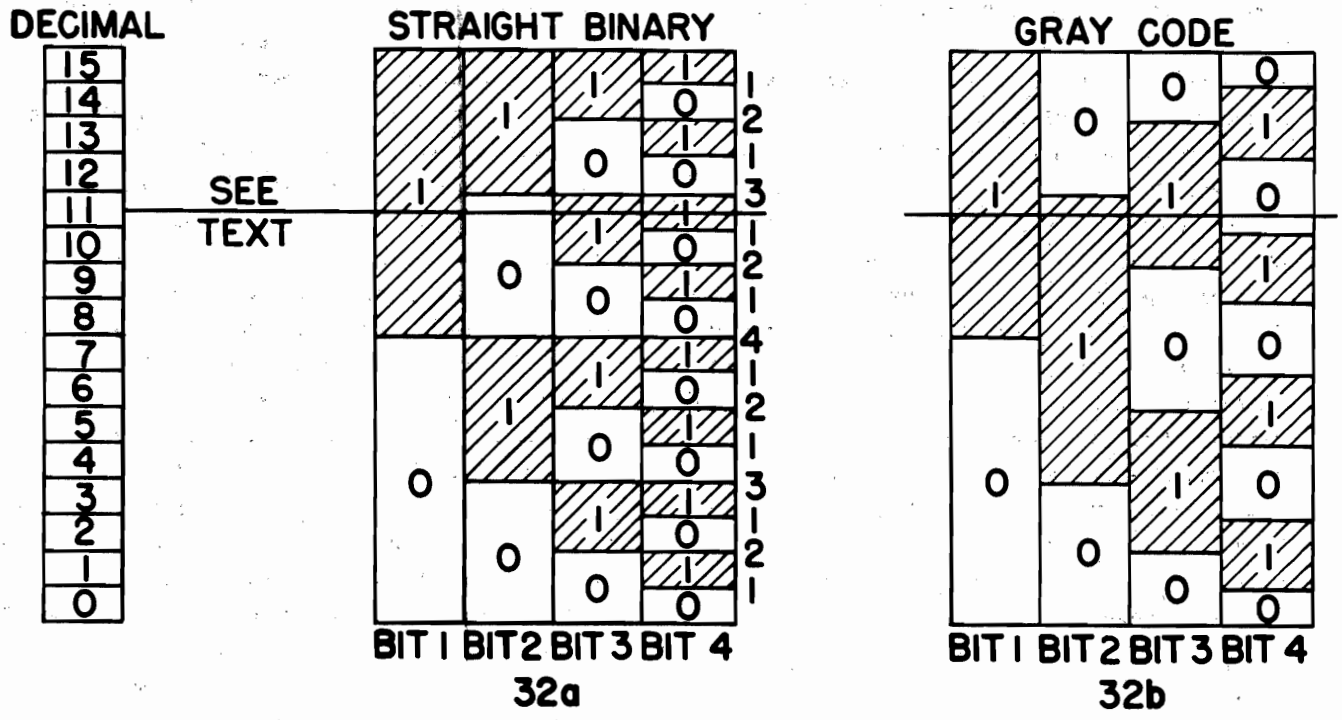


Fig. 32. Binary and Gray codes.

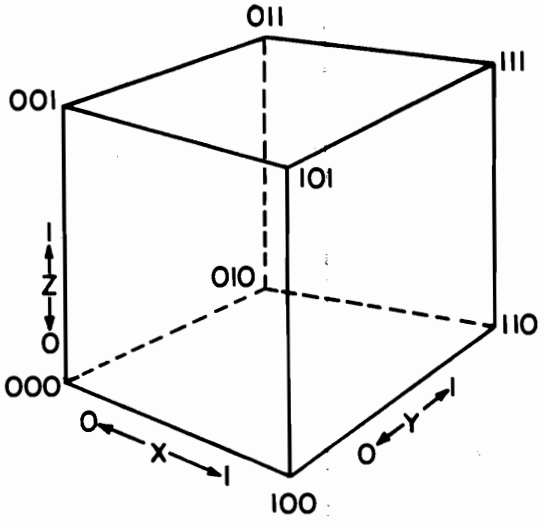


Fig. 33. Coded unit cube.

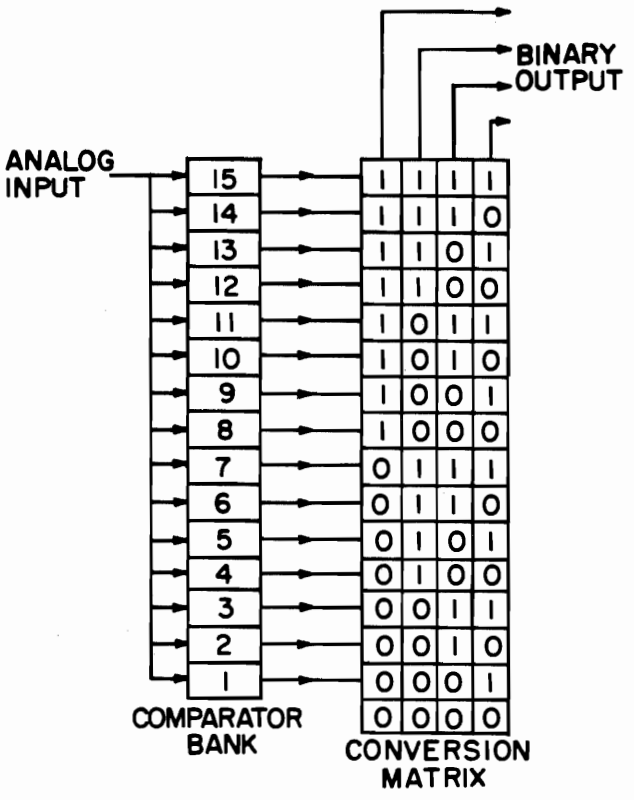
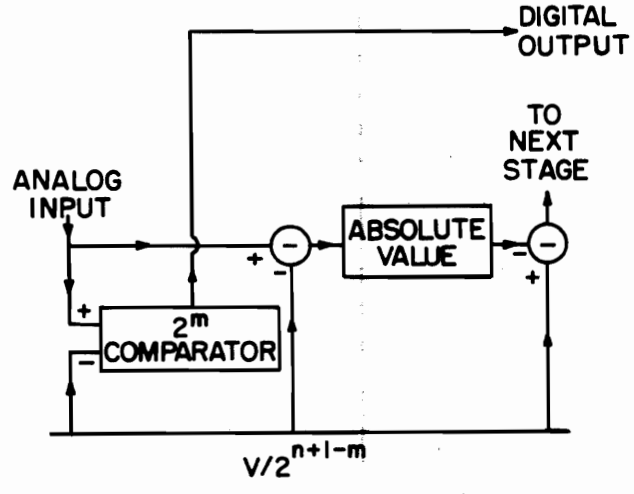
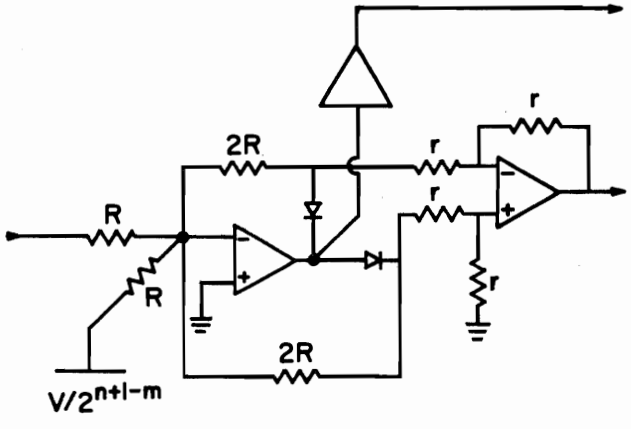


Fig. 35. Parallel ADC.



34a BLOCK DIAGRAM



34b TYPICAL CIRCUIT

Fig. 34. Sequential Gray code ADC stage.

most useful of the unit-distance codes is known as the cyclic, reflected binary, or Gray code, and is indicated diagrammatically in Fig. 32b. We note that at the eleven-unit signal level used for our previous illustration, only one binary digit is changed if the signal level changes either to 12 or to 10 units, i.e., from 1110 to 1010 or 1111. This is also true for any other signal level, as may be verified by inspection of the diagram.

Consider now our ramp function of signal input applied to a Gray code ADC. The four columns of the Gray code representation in Fig. 32b will represent the state of the outputs of the first four comparators. The first three stages of the converter must so modify the signal that comparators 2, 3, and 4 generate the Gray code shown, rather than the corresponding straight binary code (the first digit is identical in the two codes). We note first that the first comparator changes state from a 0 to a 1 output when the ramp reaches exactly half of full scale. The output waveform of the first stage is such that the second comparator changes state when the signal level reaches one quarter of full scale. However, after the signal reaches half of full scale, the first stage of the straight binary encoder subtracts one half unit from the signal and the resulting drop of the modified signal causes the second comparator to switch back to the 0 state, while the second comparator of the Gray code converter remains in the 1 state, as seen in the second column of Fig. 32b. A similar behavior is noted in the third comparator, which changes state from a 1 to a 0 when the ramp reaches one quarter scale in the straight binary ADC, but which remains in the 1 state in the Gray code device. This vertical reflection of the bit pattern of each comparator about lines at the levels of the transitions of the next higher order bit comparator may be realized by utilizing circuitry which generates a corresponding reflection of the signal at these transitions. Such a reflection of a signal about a reference level is accomplished by subtracting the magnitude of the difference between the signal and the reference level, without regard to sign, from that reference level. In circuit terms this means biasing the signal to the reference voltage, full-wave rectifying, and subtracting from the same voltage. The corresponding outputs of the first three stages of a sequential gray encoder are sketched in Fig. 31b for comparison with the corresponding outputs of the first three stages of a conventional binary encoder. By noting where each of the signals crosses the appropriate reference level for the next stage, we see that the comparator outputs will generate the Gray code pattern shown in Fig. 32b.

The functional modification of the signal which must be performed by the first stage of the Gray code ADC is

$$V_o = \frac{V_{fs}}{2} - \left| V_i - \frac{V_{fs}}{2} \right| \qquad (12)$$

where V_i is the signal input voltage to the stage, V_o is the modified output voltage, and V_{fs} is the full-scale voltage. This same function is required for each of the successive stages, with the appropriate fraction of full scale inserted in place of the $V_{fs}/2$. The block diagram of a typical stage of such a sequential Gray code ADC is shown in Fig. 34. Note that the subtractions are not dependent upon the state of the comparator, so no delay is required. For convenience, level shifts are frequently incorporated in the actual circuitry (in order to permit the comparators to make their decisions based upon zero-axis crossings of the modified signal), and x2 gain stages of the operational amplifier type mentioned in connection with the straight binary encoder are also frequently incorporated. Note that the waveforms of Fig. 31b reveal fewer high frequency components than do those of Fig. 31a, and hence that the Gray code ADC offers promise of being usable for wider analog signal bandwidths than is the straight binary ADC. A small amount of logic circuitry must be incorporated to convert the Gray code into conventional binary code for subsequent use by a computer.

The most obvious approach to fast conversion is to present the signal directly to a vast bank of comparators, separated in voltage only by the amount of resolution required e.g., five hundred comparators with 10-mV separation to achieve 0.2% resolution of signals up to 5 volts. At any given time, all the comparators below the instantaneous signal level will be in the high state and all the

comparators above the signal level will be in the zero state. Since only a knowledge of which pair of comparators bracket this transition is required, the information available from the comparator bank is highly redundant. This digital information is then converted to a binary format in a conversion matrix, as is illustrated in Fig. 35 for the case of fifteen comparator levels which produce four binary digits. This approach has not proved feasible for high resolution converters up to the present time because of the large number of active electronic components involved. However, the advent of large scale integration of arrays of semiconducting elements on small substrates may well make this approach eminently feasible in the very near future. This could lead to the realization of an "oscilloscope on a chip," analogous to the concept of a "computer on a chip" which is touted by proponents of large scale integration.

The scheme described above assumes that the comparators are of the Schmitt trigger, operational amplifier, tunnel diode, flip-flop, or similar solid-state varieties. An alternate type has been proposed which uses thin magnetic films. The signal propagates in a strip line above the surfaces of a number of patches of the film material. Each patch also carries a bias wire parallel to the signal line. The currents in the bias lines flow in the opposite direction to that in the signal line and are graded according to the current resolution required (the currents are assumed to be monopolar for this discussion). At any point on the signal waveform, all the patches where the signal current exceeds the bias current will have changed their magnetic states, while all the other patches will be in the original state. A strobe pulse applied to a strobe line across all the patches would then induce a flux-rotation pulse in the sense lines of just those patches which had been switched by the signal. The parallel sense line outputs correspond to the comparator outputs of Fig. 35. Upon termination of the strobe pulse the film patches are once more free to assume states determined by their respective ratios of signal current to bias current in preparation for the next sample.

E. Digital Memories

The very fact that we are discussing recording of transient waveforms indicates that the data in each of the recording instruments described earlier will terminate in some form of permanent storage, with the possible exception of instruments which telemeter the data to another location. In the latter case the data still ultimately find their way into a permanent memory. The telemetry may take place while the data are in either analog or digital form.

The permanent storage medium may take the form of an electronic memory contained within the recording instrument, or may take the form of a transportable medium such as magnetic tape or discs or punched cards. Machines for transcribing digital data onto the latter three media will not be considered as part of the recording instrumentation, but rather as devices for transferring data into a transportation channel. Those cases where the data are transported in analog form on tape or discs are to be considered as essentially equivalent, for our purposes, to a telemetry channel, since the data will still ultimately be digitized and stored in digital form.

The size of digital memory required is the product of the number of bits per word (for the amplitude resolution desired), the number of words or points in time, and the number of channels to be handled by the instrument. As an example, consider a recorder which is to have the same resolution as a typical oscilloscope. Such an instrument might have a signal-axis resolution of 250 tracewidths and a time-axis resolution of 400 tracewidths. This would be equivalent to 8 bits by 400 words, or 3200 bits of storage.

The speed with which the memory must operate is determined by the volatility of the previous storage medium. The speed requirement increases as we consider various recording systems in which the previous storage medium is, respectively, permanent analog storage, volatile digital storage, highly volatile analog storage, and recording in real time. Recording speed is measured in terms of the bit rate, or the product of the number of bits per word and the word rate or sampling frequency. The bit rate for the abovementioned 8-bit recorder with a 100-MHz analog bandwidth and a 200-MHz sampling frequency would be 1600 Mb/s. This is beyond the current state of the art. The conventional measures

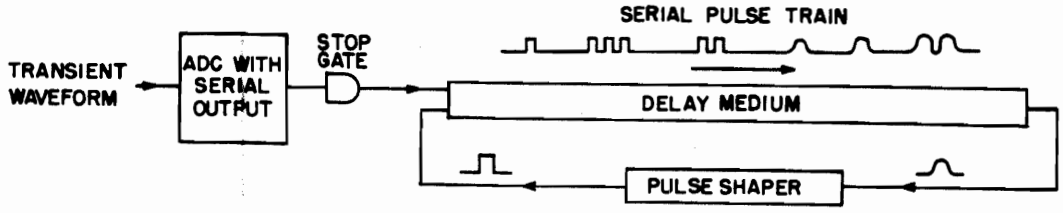
of speed associated with computer memories are not applicable to this problem. Such memories are specified in terms of their random access cycle times. These times are of little interest to us, since they differ from our situation in two ways: First, the cycle time is the time required to write a word into memory and then recall it again for use in subsequent computation, while in the transient recorder only the write time is of interest, and second, computer memories must be capable of being addressed randomly, while in our case the memory locations are addressed in a definite sequence without any need for address decoding (except possibly to reduce the component count).

For our purposes digital memories fall into three categories according to the basic manner in which data is written into them, the format in which it is stored, and how it is subsequently retrieved. The first type we may call propagating or recirculating memories. In these devices data from successive time sample points enter the medium in serial form and propagate through or along the medium, with the digital pulse shapes gradually being degraded by the dispersion and high-frequency attenuation of the propagation path. The delay time of the medium is made sufficiently long to contain the information from all sample points of the input transient waveform. At the output end of the delay medium the pulses are reshaped by electronic circuitry and fed back into the input end. The reshaping of the data pulses at each cycle obviates the distortion problem encountered in attempting to store analog data in a delay medium. The individual words or time samples may contain the entire binary description of the signal amplitude in serial form at the full bit rate as in Fig. 36a, or the memory may consist of several parallel delay lines, each containing one of the parallel bits of the quantized data and operating at the word rate as in Fig. 36b.

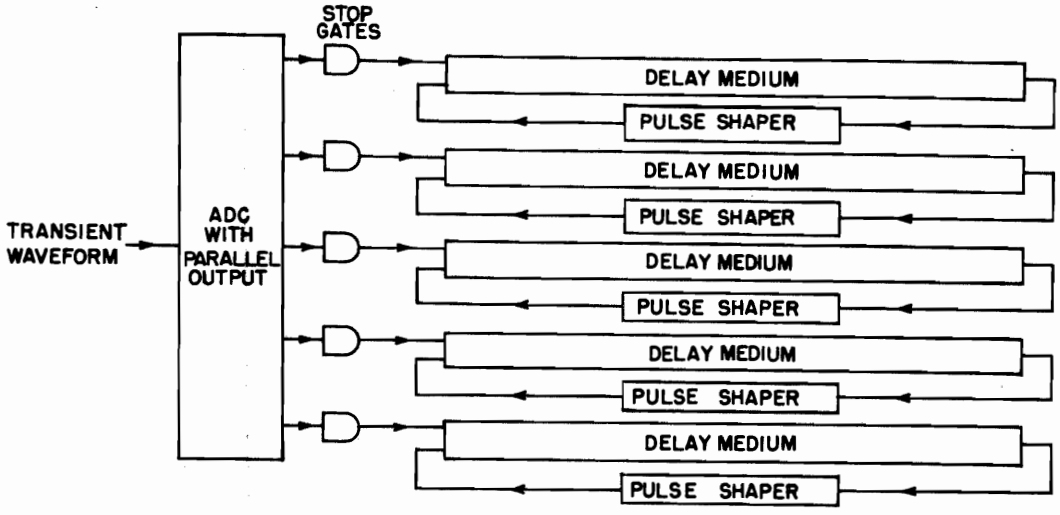
The second basic memory form consists of shift registers, which are chains of elementary bit storage elements such as flip-flops. In such a register a pattern of bits (ones and zeros) may be shifted progressively along the chain under the control of clock pulses. One complete shift register is used for each of the bit levels of the quantized data as shown in Fig. 37, with the length of each register, or the number of elementary storage locations in the chain, being equal to the number of time samples required. At the initiation of recording, the first set of parallel input data bits from the ADC are transferred into the first column of shift register elements by the first clock pulse. Successive clock cycles then cause this column of data to propagate through the register with successive bit sets of the input waveform entering from behind as the earlier words are propagated across. The bit pattern format is identical to that of the second type of recirculating memory described above, with the essential difference that by gating off the shift register clock pulses, the propagation of the bit pattern through the memory may be terminated when the data corresponding to the first point of the transient waveform reach the right-hand end of the storage register.

The third type of basic digital memory closely resembles the basic structure of computer-type memories, in that a two-dimensional array of bit storage locations is addressed by a set of bit lines and a set of word or write lines as sketched in Fig. 38. The parallel binary output of the ADC is fed simultaneously to all of the memory bit lines, so that all storage locations are potentially capable of receiving information. The word lines, however, are only addressed one at a time and are addressed sequentially so that each word line corresponds to one time sample point of the original transient waveform. Upon receipt of a word pulse, all the bit storage locations corresponding to that word line are caused to store the information present on the parallel bit drive lines. The successive word lines are addressed sequentially either by inserting a single pulse into a shift register and clocking this pulse through the register, energizing one word line driver at each of the shift register elements, or by driving the word lines from the elements of a ring counter around which a single pulse is being clocked.

Each of the above basic memory types may be used either at low speed after some preliminary waveform storage, or at high speed with a real-time ADC. The memory types in which the digital data is stored in parallel rather than in serial form are inherently better suited for the faster applications because in these devices the bit rate

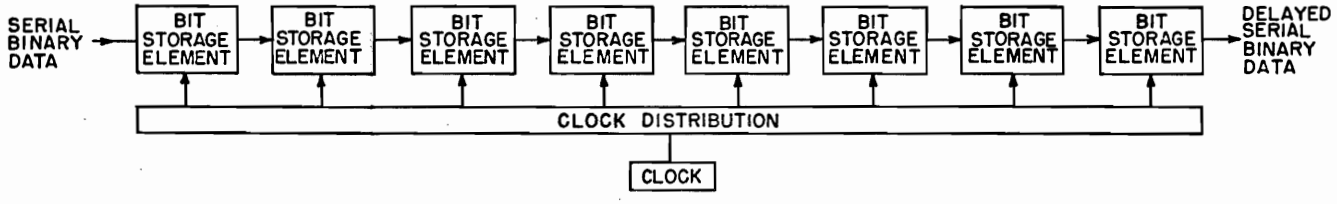


36a SERIAL DATA

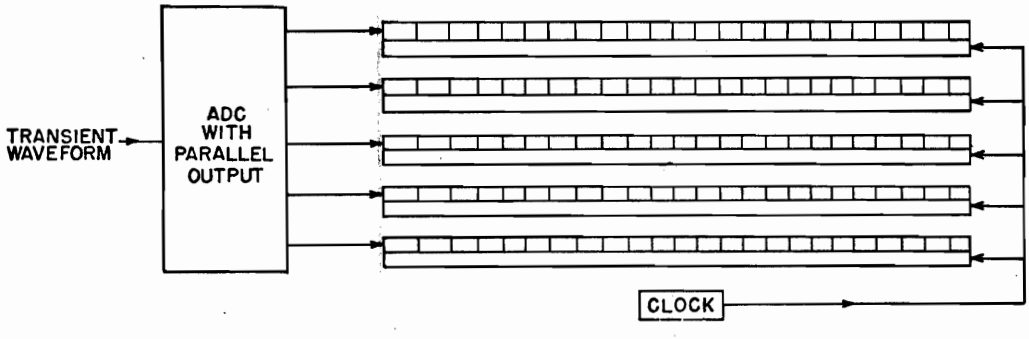


36b PARALLEL DATA

Fig. 36. Recirculating memory.



37a SHIFT REGISTER



37b MEMORY

Fig. 37. Shift register memory.

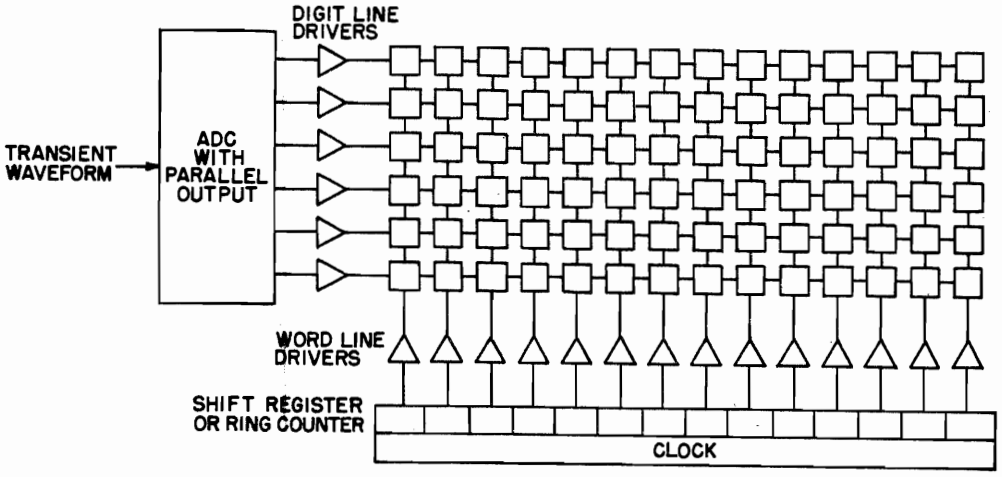


Fig. 38. Addressed memory.

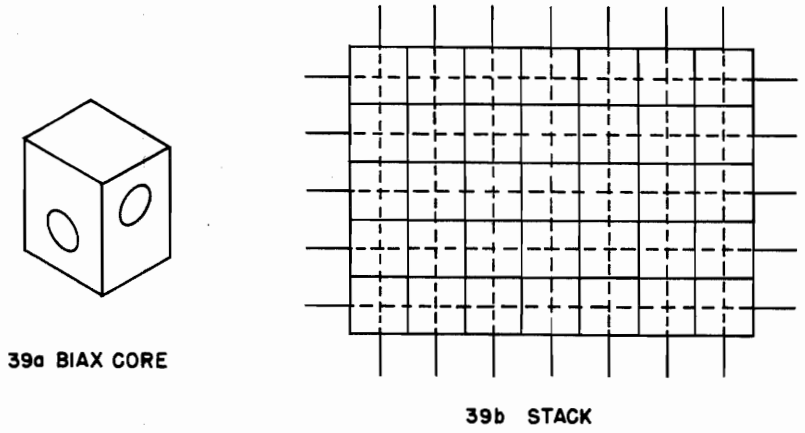


Fig. 39. Biax core stack.

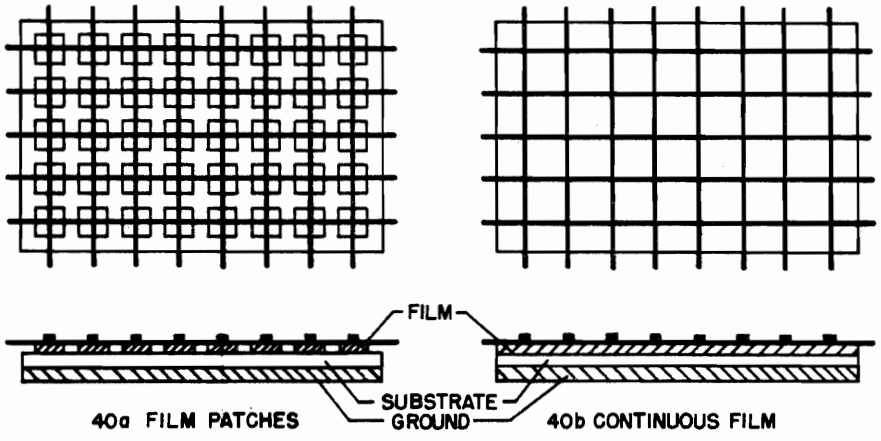


Fig. 40. Thin-film memory plane.

for each digit level is the same as the sample frequency or word rate, whereas the serial forms must work at the full bit rate.

We now turn to specific techniques for realizing the three basic memory types. The recirculating memory may use as its basic element any device in which an applied waveform may propagate independently without a need for some form of clock drive. Obviously a coaxial cable is a possible contender, but a much preferable medium would be one in which the propagation velocity is inherently slower, or one which may be packaged to occupy less space than coax. One possible approach is the use of magnetostrictive or magnetoelastic waves in a wire or rod. A transducer at the input end converts electrical pulses into mechanical waves which propagate at the sonic velocity appropriate to the medium. An output transducer then reconverts the signal into electrical form for reshaping and reinsertion at the input end. Acoustic waves have also been propagated in solid blocks of glass or quartz. Here a transducer is used to initiate acoustic pulses at one face of the block. These pulses propagate through the block and are reflected at a carefully shaped face at the other side. The angle of the far face is such that the reflected wave follows a different path from that of the incident wave. Successive reflections are caused to follow a complex pattern of propagation directions within the block by a complex pattern of facets. Ultimately the wave arrives at a second transducer which regenerates the electrical signal after an effectively long path through the block. Some of the magnetostrictive and acoustic delay media use direct propagation of the digital data pattern, while others modulate the data upon a higher-frequency carrier. Each of the techniques just mentioned may be used with different modes of transmission such as longitudinal-, shear-, or complex rotational-mode propagation. Storage of digital data on a beam of light from a laser has been accomplished by constructing a resonator of two spherical mirrors between which the light beam makes numerous passages before emerging. A resonator of this type was described earlier in connection with analog delay media. Cryogenic delay lines may also be used with digital information.

Shift registers and addressable memories may be constructed from any basic device or elementary circuit which can exhibit two different stable states, and is capable of being switched from one to the other by an applied control signal. Such devices include ferrite cores, bulk ferrite material, thin magnetic films, ferroelectric devices, cryogenic devices, tunnel diodes, four-layer PNPN devices, bistable electronic circuits incorporating active semiconductor devices, and optical devices.

Ferrite-core memories are well known through their use in computers and hence need not be discussed in detail here. The familiar arguments regarding coincident currents, inhibit lines, etc., all apply here, with the exceptions that the recorder uses simplified sequential addressing and that multidimensional memories are not required for the relatively small number of words to be recorded. Even the smallest cores are not fast enough for use with real-time ADC's, but the long word lengths available in core memories raise the possibility of storing up a few data words in an intermediate temporary storage device and hence building up longer composite words for storage at a more leisurely rate compatible with core capabilities.

There are three other techniques using ferrites which deserve mention. Attempts to achieve higher speeds with cores inevitably result in the construction of smaller and smaller sizes, with an attendant increase in difficulty in stringing them. The smaller, faster cores are now only a few mils in diameter. One attempt to alleviate this situation is the use of a solid ferrite block containing orthogonal sets of perforations through which wires are passed to form the digit, write, read, and sense lines, with the bulk ferrite material in the vaguely defined general vicinity of the intersections of these wires forming the storage elements. A closely related approach is the monolithic ferrite memory plane, in which the ferrite material is formed as a paste around a previously laid-down matrix of conductors. The third ferrite technique is to replace cores with small rectangular parallelepipeds, each containing two or more orthogonal holes. The small blocks, called Biax cores, may be stacked, with the resulting stack

resembling the ferrite block. Orthogonal sets of wires may now be passed through the holes as sketched in Fig. 39.

Thin magnetic films have been used in a number of ways for recording purposes. The resemblance of the thin-film easy-axis hysteresis loop of Fig. 20b to the ferrite-core loop of Fig. 17 indicates that the film could be used for storage using the same techniques as are ordinarily used for ferrite cores. However, the fact that switching of these films takes place by domain-wall rotation as sketched in Fig. 19 indicates that a more flexible method of writing is possible in thin films. Let the remnant magnetization in Fig. 19 indicate one of the two states of the film which we wish to utilize. A small field applied in the reverse direction will not cause the film to switch. Now a large field applied along the hard axis will cause the magnetization to rotate and lie nearly along the hard axis. Upon removal of the torque due to the hard-axis field, the magnetization will relax to the easy axis on either the left side or the right side, depending upon the direction of the applied easy-axis field. Thus, if digit-line signals smaller than the remnant magnetization are applied to the easy axis of such a film, no switching will take place until a word-line field has been used to rotate the magnetization to the hard axis and then released to allow it to fall back to the state determined by the digit-line current direction.

One application of such thin magnetic films has been in plated-wire memories. In these devices a thin film of Permalloy is plated on a copper conductor by vacuum deposition. The easy direction of magnetization of the film is caused to be circumferential by the surrounding magnetic field generated by a current passed through the wire during the deposition process. Henceforth, any current in the wire automatically creates a field in the easy axis direction, and so the wire itself becomes the bit or digit line. A second (unplated) wire wound around the plated wire can create fields axial to the plated wire and hence along the hard axis of the film. It is not necessary that the second wire actually encircle the plated wire. Instead, it may merely cross in close contact, with the small bit of film in the immediate neighborhood of the intersection becoming the storage element. Thus it becomes possible to construct a matrix of digit and word lines with storage elements at their intersections simply through the expedient of literally weaving the wires on a loom closely resembling the conventional looms used for weaving threads into fabric. More sophisticated memories may be constructed by weaving in additional separate wires for reading and sense lines.

The major limitation to high-speed operation of plated-wire memories (in common with core memories) is that the individual wires have appreciable inductive reactance and hence it is difficult to obtain rapid pulse current risetimes. This problem is alleviated in the thin-film memory plane by using the bit or word line as one conductor of a strip transmission line. In these planes the film material is vapor deposited in the presence of a magnetic field on a substrate which in turn is supported on a substantial metallic backing plane. Strip-line conductors are laid across the top of the film by techniques similar to those used in constructing printed circuits. The film area between the conductors and the ground return plane at the intersection of a digit line with a word line is the basic storage element. These elements may be deposited either in individual small patches or as a continuous film surface as sketched in Fig. 40. The digit lines and word lines above the ground plane form low-impedance transmission lines which can propagate digit or word current pulses with fast rise and fall times if properly terminated. Typical word-line currents required to rotate the film magnetization into the hard-axis direction are of the order of 500 to 800 ma. Typical digit-line currents required for reliable control of the direction of relaxation of the field upon removal of the word-line current are of the order of 100 to 300 ma. Readout is accomplished by using the word lines as read lines to rotate the magnetization toward the hard axis. The sense of the resulting rotation depends upon the flux direction stored in the film, and hence a pulse of one polarity or the other will be induced in a sense line, which may be either the original digit line or a separate line. The latter approach is preferred because a low-impedance termination is required for the digit current, while a high impedance is required for detecting the weak sense pulse, which

may only be of the order of a few millivolts. An alternate construction technique which offers promise for less expensive film memories is illustrated in Fig. 41. Here the word lines are passed through perforations in a solid stack of individual planes in a technique reminiscent of the ferrite-block memory.

Thin magnetic films have also been used in quite a different technique for construction of shift registers and other logic functions. This approach makes use of the phenomenon of domain-tip propagation. When a reverse field is applied to a magnetized film plane in an attempt to reverse the direction of magnetization, the reversal tends to nucleate at some imperfection point in the film and then to propagate across the film in the magnetization direction in a long, thin streamer which is termed the tip of the magnetic domain. In a relatively uniform film these tips tend to propagate in slightly crooked paths determined by the imperfection structure of the film. If, however, a highly conducting backing is applied close to the film and is etched into lines, the eddy currents induced in this film by a rapidly rising applied magnetic field tend to restrict the magnetic field in the film to those regions between the conducting backing lines. Hence, the domain tips tend to propagate along the spaces between the lines. By etching lines in a zig-zag pattern one can cause the domain tips to propagate in a zig-zag manner across the film and create a shift register. Other logic functions may be generated by etching the appropriate line patterns.

A storage medium similar to the plated-wire memory has been constructed using a thin tape of Permalloy wrapped spirally around a copper conductor in lieu of the plating technique. This permits realization of a nondestructive readout. After the hard-axis line of a conventional plated-wire or thin-film memory has been used to rotate the magnetization toward the hard axis to obtain a sense pulse, there is no assurance as to which direction the magnetization will assume upon termination of the read pulse if no digit-line current is present. In the tape-wound wire, called a Twistor, two layers of magnetic material are actually used. The outer layer is a so-called hard magnetic tape, and is the one in which the information is actually stored. The inner tape is a soft magnetic material whose magnetization is determined by the state of the outer layer. A read current is used which is only sufficient to cause the soft tape to switch and create a sense signal, while not affecting the state of the hard magnetic layer.

A quite different approach, but one which also uses Permalloy, is the longitudinally magnetized wire memory. In this device the wire itself is constructed of the magnetic material rather than of copper. The local longitudinal magnetic state of the wire is set by small coils wrapped around the wire or simply by tangent wires as was done in the plated-wire memory. These local magnetic states may be controlled, sensed, and shifted along the wire by appropriate sets of control coils or orthogonally woven wires.

Ferroelectric storage elements are nonlinear capacitors containing a dielectric whose relationship between electric flux density D and electric field E is similar in shape to the hysteresis loop relating magnetic flux density B to magnetic field H. Hence, the charge on such a capacitor may be switched by an applied electric field in much the same manner as the flux state of a core or magnetic film may be switched by an applied magnetic field. Thus far it has been difficult to construct ferroelectric storage elements which are stable at room temperature. Memories using these devices have not been developed very far as yet.

Cryogenic superconducting memory elements make use of the fact that the superconducting property of certain materials at low temperatures may be destroyed by a sufficiently large magnetic field. Thus, the current in an adjacent wire may be used to control the resistance of a superconducting element by controlling the ambient magnetic field. Since switching devices can form the basis of a storage element by considering their high- and low-impedance states as binary digits, we have the controllable binary element which is requisite for construction of a storage register or addressable memory.

A tunnel diode is a heavily doped semiconductor diode in which quantum-mechanical tunneling modifies the basic diode curve. With a small forward bias, excess electrons below the Fermi level and above the forbidden band in the donor region can

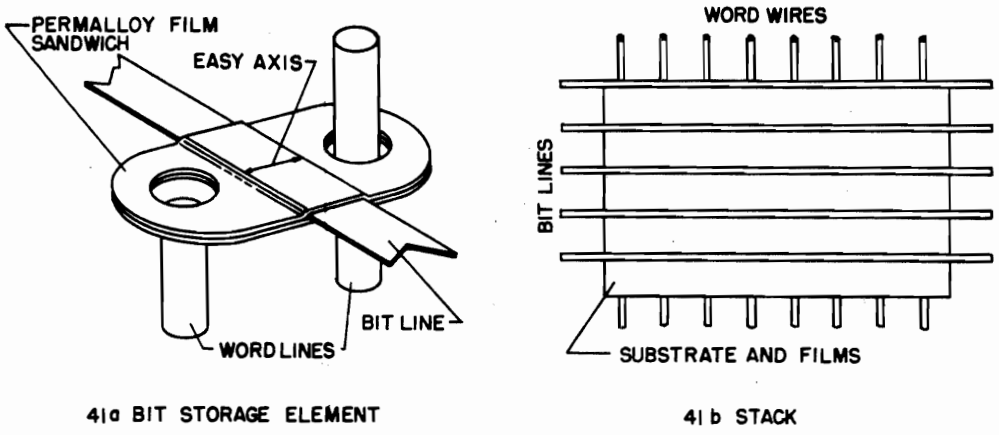


Fig. 41. Solid stack film memory.

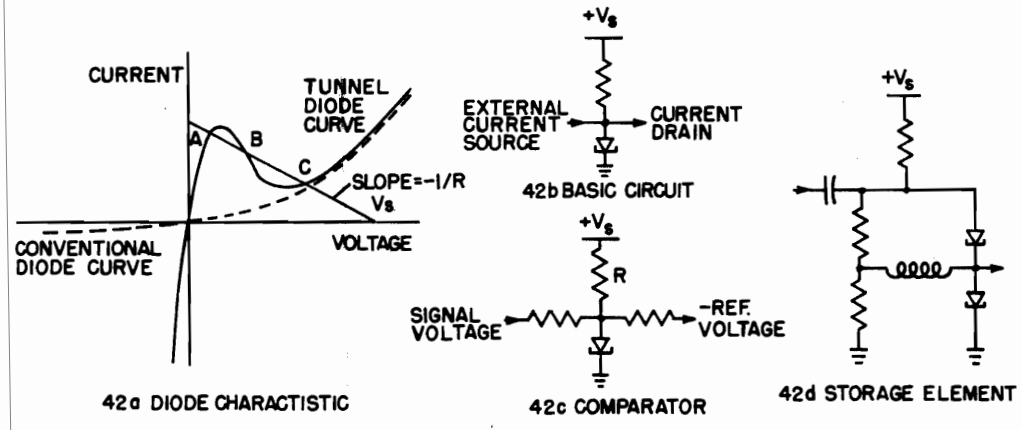


Fig. 42. Tunnel diode storage element.

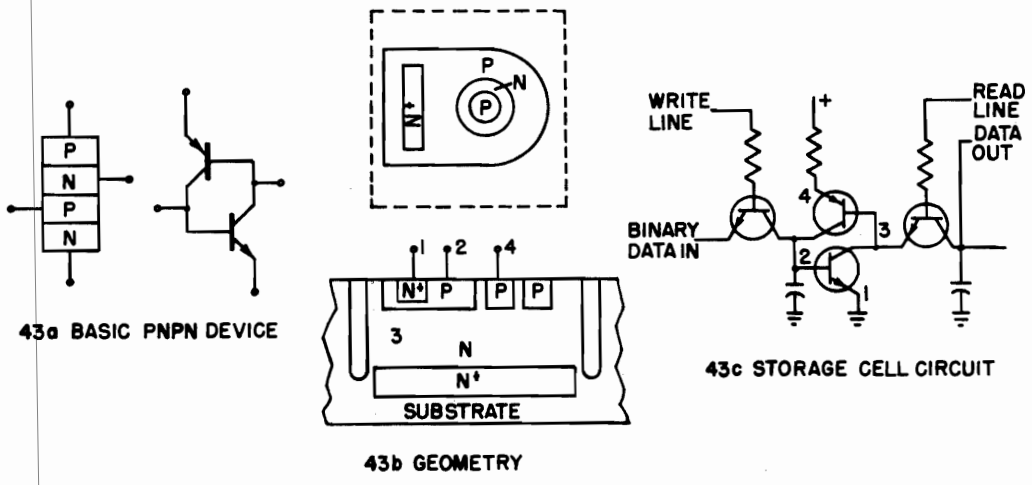


Fig. 43. PNPN storage cell.

tunnel under the barrier without energy loss to holes above the Fermi level and below the forbidden band in the acceptor region. The result is a current-versus-voltage curve of the form shown in Fig. 42a. The incremental negative-resistance region between the peak and the valley of this curve indicates that this device can exhibit two stable states when connected through a resistance to a source of voltage as in Fig. 42b. Intersections A and C of the diode curve with load line represesent stable points, while point B is unstable. If the diode is operating at point A, a small additional current supplied externally will cause the operating point to move up over the peak of the diode curve into the unstable region and then to snap to point C. The reverse transition may be triggered by a current drain which moves the operating point from point C down to the valley of the curve. This elementary circuit may be used as comparator in the circuit of Fig. 42c, where the signal and a negative reference voltage deliver currents whose algebraic sum is the triggering current. A more suitable circuit for using the tunnel diode as a storage element is sketched in Fig. 42d, where two diodes are connected in series across a supply voltage which is not sufficiently high to maintain both diodes in their high voltage states simultaneously. The result is that one diode will be in the low voltage state while the other is in the high voltage state. For use as an element in a shift register this elementary circuit is interconnected with others so that application of a clock pulse to a stage which is preceded by a stage in the one state will cause the storage element to switch to the high state, while a clock pulse received when the previous stage is in the low state will either drive the element to the low state or leave it in the low state. For use as an element in an addressable memory, the basic element is connected to receive current pulses from both the digit line and the word line which intersect at the element, with neither current alone being sufficient to switch the element but the combination being more than adequate to cause switching.

The four-layer PNPN semiconductor device is a composite structure which is essentially equivalent to two interconnected complementary three-layer bipolar transistors as illustrated in Fig. 43a. The interconnected transistor pair essentially form a complementary flip-flop, with one of its two states corresponding to current flow in both transistors and the other state corresponding to no current flow. The PNPN device is the basis of the familiar Semiconductor Controlled Rectifier, and is also frequently referred to as a "latch" circuit. Memory cells have been constructed using the geometry sketched in Fig. 43b, and seem to be appropriate for large scale integration. An experimental version containing 64 bits of storage on a single chip has been constructed. Storing and reading circuitry are incorporated as shown in Fig. 43c.

One of the most promising approaches for an addressable memory is large scale integration of storage elements constructed of bistable semiconductor circuits using essentially conventional transistors. The most common bistable circuit used is the familiar basic set-reset flip-flop illustrated in Fig. 44a. Arrays of these circuits have been constructed from discrete transistors and seem to indicate that a large integrated array is feasible. The major differences between types of storage elements which have been proposed are in the details of the associated writing and reading control circuits. Most of the memories which have been proposed are intended for use in computers and hence are optimized for random-access addressing. Hopefully, the fact that we only require a simple sequential addressing scheme could lead to less expensive integrated memories, or to the possiblity of incorporating larger numbers of storage elements on single chips. A variety of relatively small integrated arrays of storage elements have been constructed for use primarily as read-write, scratch-pad memories. One typical such unit consists of eight bits of storage with complete address decoding (from a three-bit address word) and input-output buffering on one chip. This device, sketched in Fig. 44b, is intended to provide one bit for each of eight words, with the number of bits to be used in a word being made up by incorporating the appropriate number of chips. Arrays of these chips would then be used to construct memories of larger numbers of words. Another device, whose basic circuit is sketched in Fig. 44c, incorporates sixteen bits of storage with write-line drivers and sensing amplifiers, but brings out the separate write lines more nearly

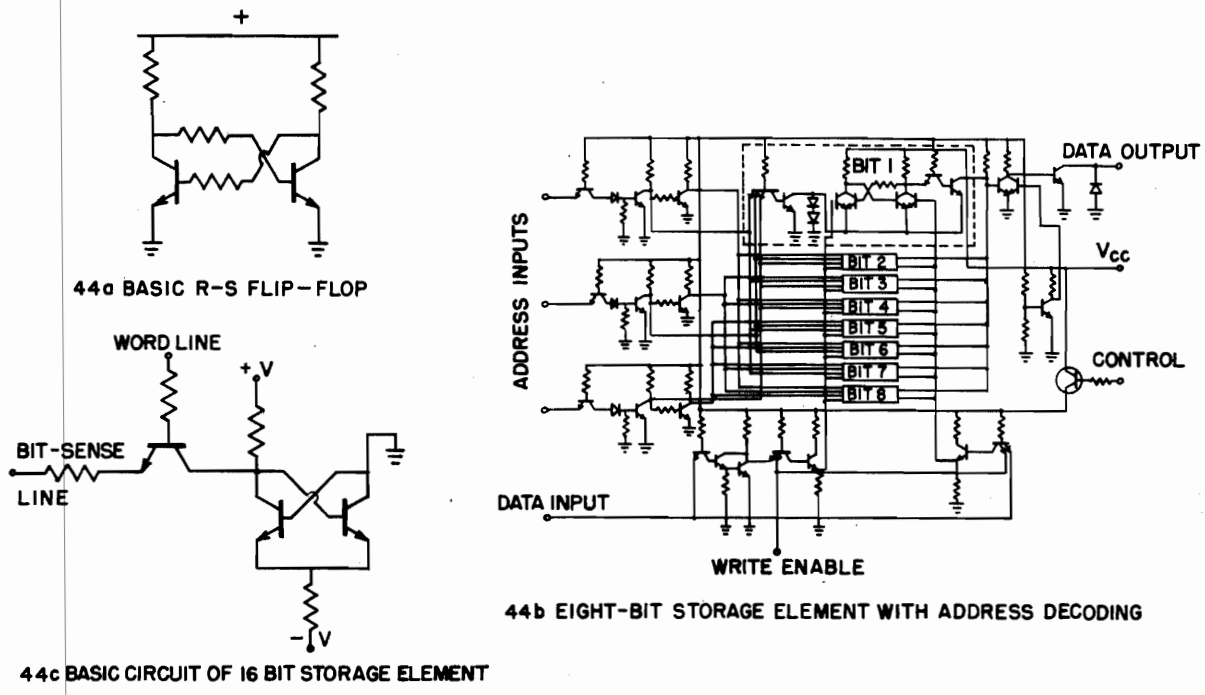


Fig. 44. Bipolar memory cell.

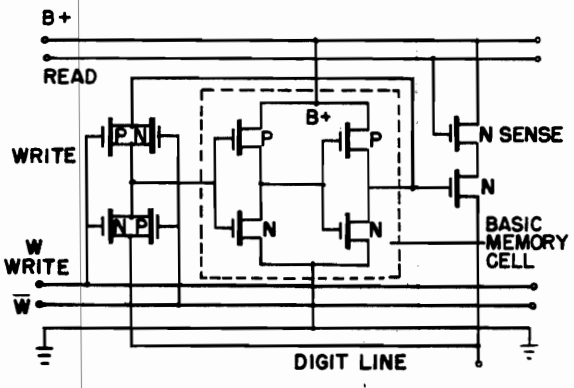


Fig. 45. MOS memory cell.

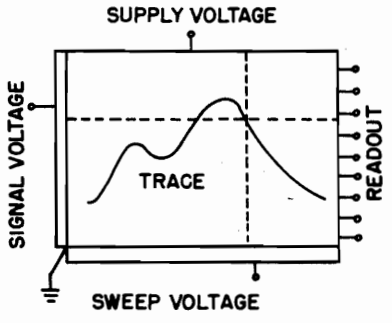


Fig. 46. Ideal analog-addressed memory.

in the manner which would be required for our sequentially addressed memory. Another manufacturer has announced that a 32-bit device will be available shortly. There seems to be no particular reason why integrated circuits large enough to comprise the complete memory for a transient waveform could not be constructed if there were sufficient economic justification.

Much larger scratch-pad memories have been constructed using insulated-gate field-effect transistors (IGFET's, MOSFET's, MOST's or MISFET's). These devices are much better suited to large scale integration than are bipolar transistors, but do not at this time have the speed capability of the latter, and hence, for the time being, are limited to word rates of the order of a few megahertz. The basic storage element of a typical complementary MOSFET memory cell with its digit and word line connections is shown in Fig. 45.

A complete integrated memory would also include the addressing shift register or ring counter shown in Fig. 38 because this would eliminate the need for bringing a separate lead for each word line out of the package.

One of the basic limitations of the addressed memory in the form which we have been discussing is the need for separate leads to each of the discrete word lines and digit lines. For a memory large enough to provide good time resolution of the transient waveform, the number of word lines may approach 1000. For a fast memory for real-time recording, each of these drive lines must be constructed as a coaxial or strip transmission line, with the attendant constructional difficulties. It would be far better if a scheme could be devised using a non-ordered matrix of memory cells (at least for the write function). By a non-ordered memory we mean one in which any given physical location on a nearly continuous storage surface may be addressed simply by two analog voltages, one for each of two orthogonal axes. Such a storage surface would have many more resolvable elementary storage locations than the minimum number of discrete storage cells used in the types of addressable memories discussed above. The non-ordered storage surface has a tremendous constructional advantage over discrete elements, in that it can be made from bulk semiconductor material rather than being composed of many individually designed elementary circuits, each requiring several masking steps and layers of different materials. It also avoids interconnections, which are the nemesis of most integrated circuits. The signal-amplitude axis could in this case revert to being a continuous range of analog voltages, rather than requiring an ADC to supply parallel binary information. As the point represented by the two voltages swept across the surface tracing out the waveform, the unordered cells which were excited would change state to record successive points on the transient waveform. Typical examples of non-ordered memory surfaces are the phosphor screen of a cathode-ray tube and the storage target of a scan converter. These devices per se, however, are not of interest for this part of our discussion because here we are seeking alternatives to the use of large fragile vacuum envelopes and high-voltage power supplies. What one would really like to have is a small semiconductor device (about the size of present-day integrated circuits) in which a physical storage point is defined by a pair of analog voltages supplied to two pins as sketched in Fig. 46. Discrete readout digit and word lines would be acceptable in such a device because it is assumed that readout would be accomplished at a much-reduced rate and hence lead configuration would not be a problem. A still better scheme would be one in which readout is accomplished in a binary manner on both the amplitude and time axes, with an attendant reduction in the number of leads required, e.g., ten lines for binary representation of 1024 time points. Note that rather than being a digital memory, this hypothetical device has become essentially a solid-state scan converter with digitization during readout. Although such devices are not available at the present time, much research is underway in attempts to find a way to address locations in a non-ordered plane by means of a pair of analog voltages. Such a capability is needed, for instance, in developing solid-state equivalents of television camera tubes and cathode-ray display tubes or television picture tubes.

An alternative approach, which is less desirable than the pure analog addressing scheme, but which would still be preferable to the use of discrete digit and word lines, would be a memory plane

containing a discrete array of storage elements as in the addressable memories described above, but in which addressing is accomplished by two voltages which must take on discrete step values. Readout could be accomplished either by a similar set of digitized word- and sense-voltage levels or by discrete physical leads. Three types of memories operating on this or related principles have been developed for use in computers. These devices use minute electron beams or light beams and hence do not satisfy our criterion for a completely solid-state device, but are included as illustrations of the analog-selection principle (in the hope that they may encourage further speculation in this direction). The first involves the use of an analog-deflected electron beam which is used to store a positive charge pattern on the surface of the insulating layer of a MOSFET (much as is done in the storage target of the scan converter). The basic memory plane would be an array of MOSFET's arranged in rows and columns and interconnected with readout word and digit lines. This device has the disadvantage of the high-voltage electron beam of the scan converter, but has the advantage of employing solid-state readout rather than a read gun.

The next device of interest writes with a laser optical beam on a storage plane constructed of a magneto-optical material such as manganese bizmuth or crystalline gadolinium-iron-garnet. Writing is accomplished by deflecting the laser beam to the selected address, using the high power density of the beam to raise the storage element above its Curie temperature, and then allowing the spot to cool in the presence of an external magnetic field which sets the direction of magnetization assumed by the storage element. Readout is accomplished by using a lower-powered, polarized light source and detecting the direction of Faraday rotation of the beam by means of an analyzer plate and a photodetector. Two orientations of polarization are used to correspond to the binary high and low states.

Another optical approach uses a ferroelectric optical ceramic material such as zirconate-lead titanate, barium titanate, or sodium potassium niobate for the storage plane. The domains of coarse-grained polycrystalline ceramic act as though they were composed of thin flakes of opaque optical material. In the presence of an electric field in the direction of the thickness of the plane, the domains tend to become aligned with the electric field and hence to permit light transmission through the plane. An electric field applied in the plane of the surface tends to align the domains so as to block light transmission. Memory cells are constructed by applying a matrix of electrodes to both sides of the storage plane so as to permit application of either axial or transverse electric fields. The ferroelectric property of the ceramic material permits an electric flux to remain in the absence of an applied field and hence causes the domain orientation to be maintained after removal of the field. This device is one in which readout is optical but in which writing is accomplished in the same manner as in the digital memories described earlier, i.e., via sets of digit and word lines. Since information is stored in the form of transmission or lack of transmission of light, readout may be accomplished either by directing a light beam to the appropriate sequence of memory cells and detecting the light transmitted to a photocell on the other side of the plane, or by illuminating the plane uniformly and detecting the light received in a matrix of photodetectors associated one-to-one with the memory cells. In principle, a matrix of semiconductor photodiodes could be integrated in a plane to be mated with the ferroelectric plane, and interrogated by a set of word and bit reading lines. Such a memory would have the characteristics of some of the discrete semiconductor digital memories described above, with the advantages that the basic storage medium is a non-ordered material with its associated ease of construction, and that there is a separate readout matrix composed of relatively simple elementary photodiodes.

V. EXAMPLES OF STATE-OF-THE-ART RECORDERS

In order to assess the width of the gap between the transient waveform recording objectives outlined in this report and the current state of the art, a few examples of existing and forthcoming recorders employing the principles we have discussed are presented below. Some of these represent complete recording systems, while others are constituent assemblies which could be incorporated

in larger systems.

The scan converter, while not meeting the objective of being a compact device, has the distinction of having been developed into a relatively practical working instrument. A scan converter tube of the type pictured in Fig. 47 has been packaged, together with its associated writing and reading electronics, power supplies, calibrators, and telemetry signal conditioning, into an instrument which has been flown in a rocket instrumentation package and dropped in a parachute-drogued drop package. The traveling-wave-deflection version of this tube, which was developed jointly by C. U. Benton of the Los Alamos Scientific Laboratory (LASL) and the Rauland Corp., has a bandwidth approaching 10 GHz, a resolution of approximately 800 lines, a sensitivity of ±80 volts for full signal-axis deflection, and may be subjected to more than 100 G's and 14,000 gamma roentgens without physical or image degradation. An example of a 20-nanosecond pulse as seen on a playback monitor is shown in Fig. 48. Note the excellent writing rate in the leading edge of the pulse. At least two major instrument manufacturers are developing laboratory instruments which use the scan converter as the basic recording element for fast transients. In these instruments a visual display is obtained by playing back the output of the read side of the scan converter on an inexpensive conventional cathode-ray tube. In this manner, the writing-rate limitations of conventional oscilloscope tubes are overcome, and the recorded waveform is available for viewing as many times as are desired, simply by repetitive scanning of the stored waveform by the read gun.

The DEMEX system being developed by EG&G, Inc., (Bedford), with consultation by LASL personnel, for the Defense Atomic Support Agency (DASA) is a typical example of a solid-state transient recorder. Its block diagram is shown in Fig. 49. The input waveform is applied simultaneously to sixteen transistor-driven tunnel diode comparators. The redundant comparator outputs are buffered and feed sixteen parallel bit line drivers which drive sixteen parallel digit lines in a Texas Instrument thin-film memory plane. A continuous-film memory plane is used rather than one incorporating individual storage element patches. The word lines are driven sequentially at a 100-MHz rate by a shift register. Readout is accomplished by driving the same word lines by the shift register at a greatly reduced rate, with the stored information appearing on a separate set of bit sense lines. Since destructive readout is used to obtain reasonable sense output levels, a read-and-restore cycle is used, in which reading is accomplished on the rise of the word-read pulse, and rewriting is accomplished on the fall of the same pulse. The memory capacity is 256 words of 50 bits each, which permits the simultaneous recording of three transient waveforms, with two bits of each word available for housekeeping information. It would be a relatively simple matter to modify this system to include a larger number of comparators with a conversion matrix to translate the redundant comparator outputs into binary information. The existing memory capacity could then handle six channels, each with a resolution of eight bits, or one part in 256. This recorder has been designed for used under rugged environmental conditions. It is capable of withstanding the acceleration, vibration, and temperature rise of a rocket instrumentation section. The instrument has been hardened to withstand a radiation environment, and hence some portions of the electronic circuitry realize somewhat less performance capability than could be designed into them. The data read out of the thin-film memory plane are both telemetered to the ground and written on a ruggedized 250-kHz tape recorder on board.

A faster sampling system using analog storage is being constructed by the UNIVAC Corp. for DASA. The sample width is one nanosecond, with an effective repetition period of one nanosecond and a total of 30 samples. The signal propagates down two short lengths of segmented delay line and is sampled by strobed diode-bridge gates as seen in Fig. 50. The resulting samples are held temporarily on capacitors. After a delay of 200 nanoseconds, the samples are stored in analog form in transfluxors during the next 200 nanoseconds. Readout is accomplished by a sense winding which passes through the small aperture of the transfluxor and through a balancing transfluxor used to cancel out nonlinearities.

Gralex Industries, Inc., composed of former personnel of Marquadt Industrial Products, Inc.,

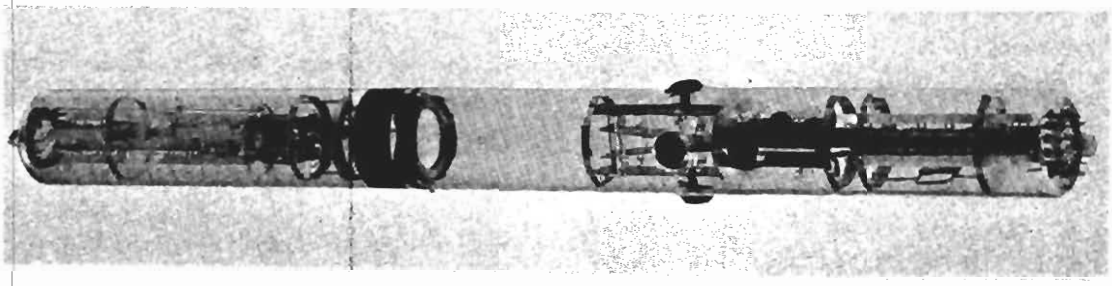


Fig. 47. Scan converter tube.

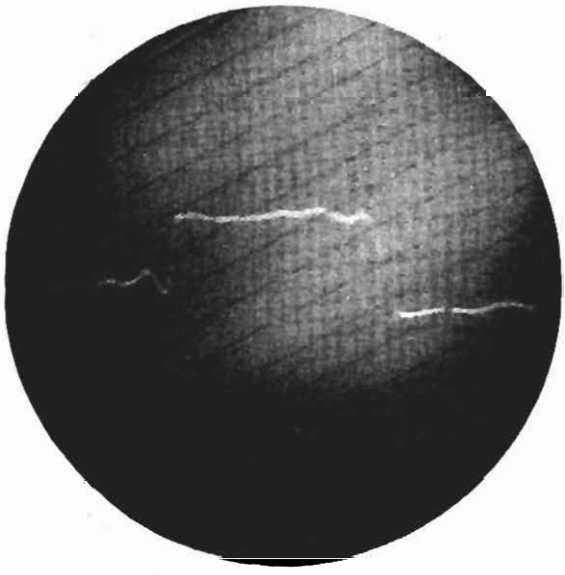


Fig. 48. Twenty-nanosecond pulse on scan converter.

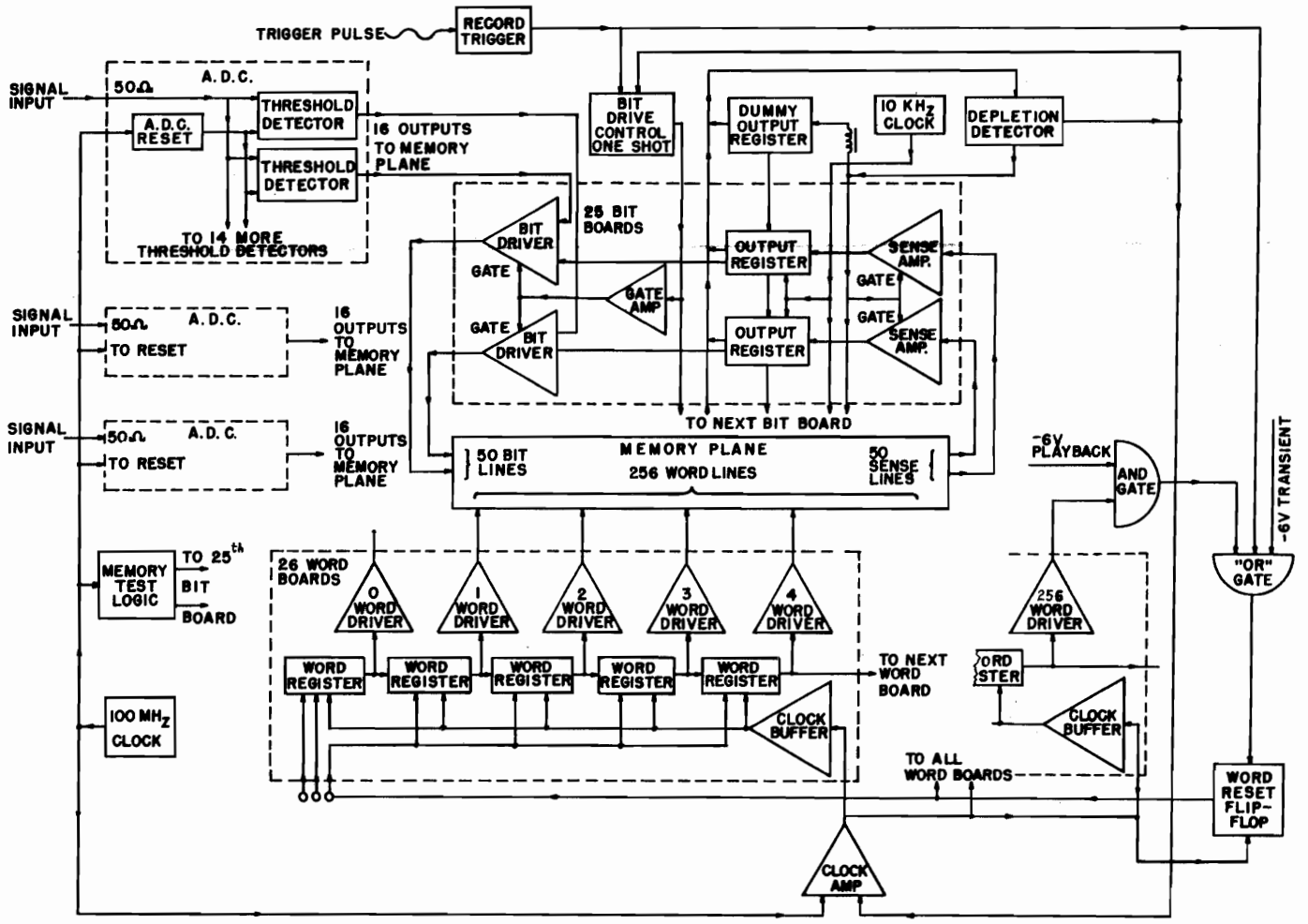


Fig. 49. DEMEX block diagram.

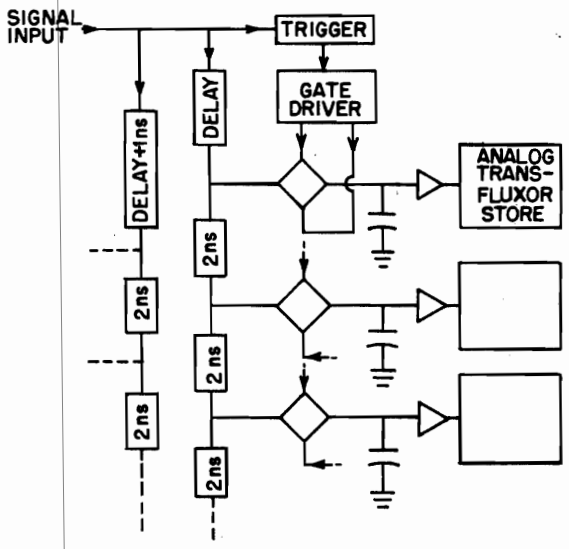


Fig. 50. UNIVAC gigahertz analog sampler.

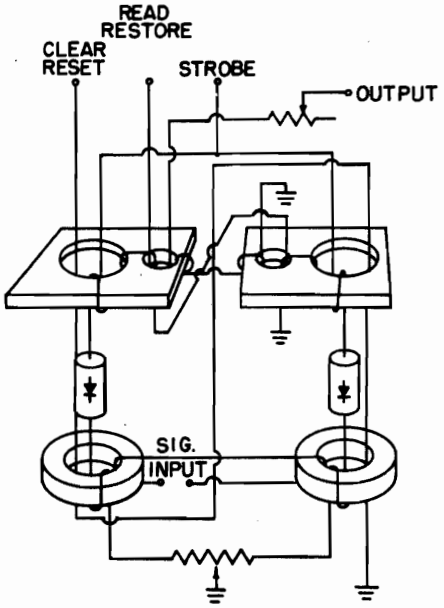


Fig. 51. UNIVAC TRED stage.

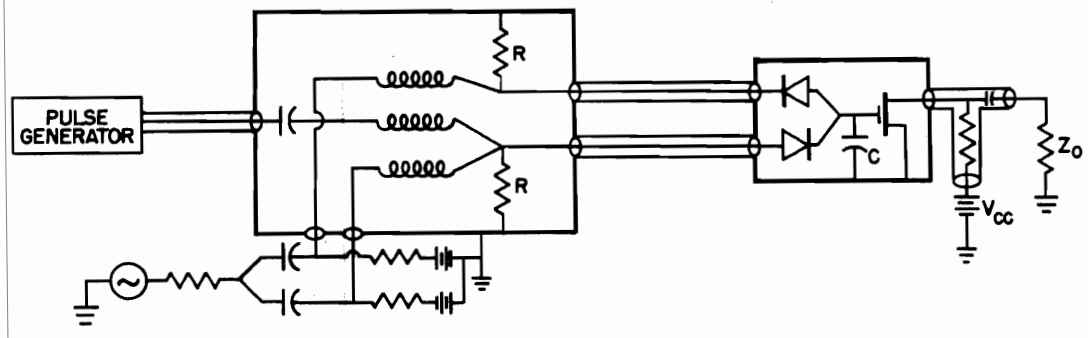


Fig. 52. BTL VHF sample and hold circuit.

formerly General Applied Science Laboratories, Inc., markets a modular sampling transient recording system. This system uses the approach of applying the signal simultaneously to a large number of sampling heads and strobing the samplers successively. The individual samplers are independent of one another, and as many samplers may be incorporated as are desired to define the waveform. The minimum available sample width is one nanosecond, and the interval between samples may be as short as 0.1 nanosecond. A family of modular components such as trigger circuits, trigger regenerators, strobe delays, strobe pulsers, and analog storage units is available for building up a system of any desired degree of complexity. At the present time the individual modules are larger than might be desired for a field system, with at least a full relay rack being required for a typical system. The individual samplers consist of transformer-driven diode-bridge gates, with the sample being stored on a capacitor at the grid of a nuvistor vacuum tube. The vacuum tube may be used to charge a second capacitor for longer analog storage, if so desired.

The Illinois Institute of Technology Research Institute has proposed a system in which the signal is sampled and stored for a short period of time on a capacitor and then transferred to multitrack magnetic tape or drum storage. The individual tracks have the bandwidth of typical modern high-speed analog tape recorders, i.e., ~ 1 MHz, and a large number of parallel tracks are used, one for each time sample of the transient waveform. Alternatively, a smaller number of tracks may be used, with the first few successive time points being recorded on successive tracks across the tape, but with the capacitor storage being deliberately made sufficiently volatile that after a sample is placed on the last track the commutator can return to the first track and then repeatedly scan the tracks for successive groups of time samples.

In 1964 personnel of the United Kingdom Atomic Weapons Research Establishment constructed a five-bit recorder using the fanout approach, except that individual ADC's were used for each sample. The repetition period was ten nanoseconds.

EG&G, Inc., (Santa Barbara) is constructing a recirculating optical system, components of which have been mentioned earlier in this report. This system uses an optical delay line to store the complete signal waveform. A small fraction of the modulated light beam is permitted to escape through a partially silvered mirror on each pass and is then detected by a photomultiplier whose output is sampled with a time period slightly longer than the time for one complete cycle through the optical resonator, so that successive sample points effectively appear at progressively later and later points on the waveform.

EG&G, Inc., has also constructed several versions of a specialized sampler called a Sampling Transient Analyzer, which is essentially a segmented delay line type of system. This recorder is somewhat specialized in that it is optimized for exponentially rising signals, and hence must operate over a very large dynamic range. This range may be accommodated in either of two manners: A fixed fractional attenuation may be inserted at each segment of the delay line in order to supply approximately equal signal levels to the samplers (assuming that the exponentiation rate is approximately the predicted value), or the samplers may be optimized to sample larger and larger signal levels along the length of the segmented line. Both approaches have been used.

A radiation-hardened recorder called TRED, standing for Transient Radiation Effects Detector, was constructed by UNIVAC for Boeing. This recorder uses the magnetic modulator principle which was described earlier in connection with sampling gates. The signal is impressed upon a segmented delay line which has its center conductor passed through pairs of magnetic modulator cores at the segment junctions. The signal current varies the inductance of the modulator cores, and thus modifies the magnitude of a strobe pulse which is passed through the modulator cores and through a pair of transfluxors operated in push-pull. The frequency response or risetime of such a system is limited by the rate of flux propagation in the modulators and/or the transfluxors. Readout is accomplished either by means of sense windings passed through the small apertures of the transfluxors, or by incorporating the core in an oscillator circuit whose frequency is determined by the inductance of the unsaturated portion of the core. One sample-and-store stage is shown in Fig. 51.

A number of fast sample and hold circuits are available. R. E. Fisher of the Bell Telephone Laboratories has designed a coaxially coupled version of the transformer-coupled half bridge which is capable of a 720-Mb/s bit rate based on a 6-bit word at a 120-MHz sampling frequency. This unit was designed as a companion to an ADC to be described later. The circuit of this unit is sketched in Fig. 52.

J. R. Gray and S. C. Kitsopoulous of the Bell Telephone Laboratories have designed a diode-bridge sampler which operates an order of magnitude slower (12 MHz) but is capable of a precision of 9 bits. This high precision is achieved by use of a balanced drive for the bridge and the use of carefully matched diodes.

E-H Laboratories, Inc., markets a strobing voltmeter which is essentially an S&H circuit. The signal to be studied passes in and out of the instrument and is strobed at a time controlled by a separate strobe pulse input with an appropriate delay. The single sample, which may be as short as 5 nanoseconds, is stored for as long as is desired and may be displayed on a conventional voltmeter. This unit is physically large in the marketed version, but the critical internal sampling elements could be packaged more compactly for a system which would employ a large number of strobed S&H's.

There also are a number of commercial ADC's available. Bunker-Ramo markets an 8-bit sequential Gray code ADC of the type discussed earlier in this report. This unit is capable of quantizing a bit within approximately 40 nanoseconds after the time the input signal settles. This company has done further work on this type of converter and has developed faster units which have not yet reached the public.

An ADC which was originally developed for the NIKE-X program by Western Electric is now being marketed by Computer Labs, a company largely comprised of personnel who formerly worked on the Western Electric project. These converters are capable of supplying either Gray or binary code at a rate of 9 bits at 2.5 MHz, 7 bits at 5 MHz, 5 bits at 10 MHz, or 4 bits at 12.5 MHz of analog bandwidth.

Personnel of the Sandia Laboratories have developed a fast tunnel diode comparator bank which could be combined with a binary converter to make a fast ADC. This unit may be operated without degradation of parameters over the temperature range from -20° to +70° C with a simultaneous neutron irradiation of 10^{15} nvt.

R. E. Fisher of the Bell Telephone Laboratories at Murray Hill has developed a 1200-Mb/s, Gray code, ADC which furnishes an output not in the form of current pulses, but rather as phase reversals of a 9-GHz microwave carrier. The 1200-Mb/s equivalent bit rate corresponds to 6 bits at a 200-MHz sample frequency.

Two other agencies have developed 5-bit converters working at 200-MHz word rates with conventional binary output in the form of current pulses.

Bipolar integrated memory cells at the medium-scale level of integration for use in scratch-pad memories are available from Sylvania, Transitron, Motorola, Fairchild, Signetics, Texas Instruments, and International Business Machines (IBM). Fairchild offers a complete scratch-pad memory which may be built up from their units. A number of other manufacturers offer scratch-pad memories built up from individual small-scale integrated circuits. Medium-scale integrated arrays of MOS elements suitable for incorporation in scratch-pad memories are available from the Nippon Electric Company, the Radio Corporation of America, General Micro-Electronics, Philco-Ford, General Instrument Corp., Fairchild Semiconductor, American Microsystems, Westinghouse Aerospace Division, Westinghouse Molecular Electronics Division, and Texas Instruments. Thin-film memories are available from Texas Instruments, Burroughs, Fabri-Tek, UNIVAC, IBM, and the Librascope group of General Precision, Inc.

VI. NEW DEVICE DEVELOPMENTS

Since the advanced transient waveform recorders which one would like to design are slightly beyond the state of the art of the present time, it is necessary to consider not only all new techniques which are proposed, but also to make use of any available new devices, particularly devices which offer a speed advantage over existing semiconductors. A number of new device developments which have appeared within the past few months are described below.

S. Sze and M. Lepselter of the Bell Telephone Laboratories have recently announced construction of a new type of Schottky-barrier diode using a beam-lead construction technique. This device exhibits a reverse recovery time of the order of picoseconds (not measurable by today's techniques), and a reverse breakdown voltage as high as 450 volts. The construction technique used makes it feasible to build such a diode integrally across the base-collector junction of a transistor for use in extremely high speed nonsaturating logic.

Hot-carrier diodes are the favored devices for construction of diode-bridge samplers and for general fast rectification applications. However, these devices generally exhibit a low reverse voltage capability ($\approx$ 30 volts), and are relatively expensive. A new approach to diode design and assembly by Hewlett-Packard Associates results in a new hybrid diode which combines the picosecond switching speed and low-voltage turn-on of the hot-carrier diode with the low leakage, ruggedness, and uniformity of the conventional silicon PN junction diode. The new construction technique also results in a drastic cost reduction, with the new devices being priced well under one dollar, as compared to five to ten dollars for conventional hot-carrier diodes. Typical effective minority-carrier lifetime for these diodes is of the order of 100 picoseconds, and their breakdown voltage is 70 volts minimum. Presumably new and better additions to this line will be forthcoming shortly.

It has been recognized for some time that diodes connected across the collector-base junctions of transistors to prevent saturation can increase the speed of switching circuits by minimizing the minority-carrier storage in the base regions. The most recent discrete circuits have used Schottky-barrier diodes to fulfill this function because of their fast switching times. Up to now it has not proved feasible to integrate this type of diode with a transistor. Recently, however, researchers at the Electrotechnical Laboratory of the Japanese government have succeeded in constructing TTL logic circuits with integrated Schottky diodes. The technique has not been pushed very far as yet, but even the preliminary attempts succeeded in speeding up conventional TTL circuits to the capabilities of the faster circuits available on the market today.

E. S. Schlig and C. A. Baskin of the IBM Watson Research Center have recently investigated the enhanced speed capabilities of germanium emitter-coupled logic circuits at low temperatures. They have succeeded in developing picosecond-range integrated circuits with potential advantages in power dissipation, noise immunity, and reliability. The cryogenics requirements are not severe (-100°C). Silicon devices tend to perform less satisfactorily at low temperatures, while the germanium devices indicate an increasing f_t as the temperature is reduced from room ambient to -100°C. The average logic delay exhibits a minimum ($\approx$ 300 ps) at -100°C.

One of the factors which limits the high-frequency performance of conventional transistors is the inability to use high doping levels in the base region because of the relatively narrow band gaps of germanium and silicon. It has been recognized for many years that availability of wide-band-gap materials such as gallium arsenide would permit the use of heavier doping with a corresponding improvement in high frequency performance. Up until recently, it has not been possible to construct devices using these wide-gap materials because of trace chemical impurities. Recently Professor D. L. Feucht, A. G. Milnes, D. K. Jadus, and H. J. Hovel of Carnegie-Mellon University have succeeded in controlling the contamination level through the use of ultra-clean-room conditions, and have successfully constructed transistors of gallium arsenide with germanium and of zinc selenide with germanium.

It will be noted that throughout this report MOS field-effect transistors and bipolar transistors have been treated separately because of the difficulty of fabricating these two types of devices on the same substrate. Recently, R. Lyer of the Westinghouse Molecular Electronics Division has succeeded in combining a P-channel MOS device and an NPN bipolar transistor on the same chip. This development offers great promise for future integrated memory arrays and logic.

Motorola has recently introduced the first units in its widely heralded MECL III emitter-coupled logic family. These devices have risetimes of approximately 0.4 nanosecond and propagation times of approximately one nanosecond. The only devices

marketed so far are a dual four-input gate, a quad two-input gate, and a master-slave flip-flop. Within a few months, more interesting devices for our purposes, such as a scratch-pad memory array and a shift register, should be available. In all probability other manufacturers will follow suit shortly.

UHF field-effect transistors have been available for some time, but recently two manufacturers have announced production of microwave FET's. Siliconix has available a junction device with a transconductance of 6,500 micromhos and a usable frequency range of 1.5 GHz. Fairchild Semiconductor has taken quite a different approach. The gate element of their device is a Schottky-barrier diode on an n-type gallium arsenide film. This device has exhibited a gain of 10 db at a frequency of 1 GHz and is reputed to be capable of being modified to push its frequency limit above 10 GHz.

A new class of circuits may become available through use of a characteristic of diodes which normally is considered undesirable. The high frequency limitation of conventional diodes is caused by charge storage in the junction. However if, for very short times, the diode is treated as a charge rectifier rather than as a current rectifier, a new class of circuit concepts becomes available. Using these concepts, shift registers, serial memories, and other pulse and logic circuits have been proposed.

Another development, in a somewhat different vein, is a wide-band high efficiency optical modulator. It was mentioned earlier that the optical modulator was one of the limitations of several optical schemes which have been proposed. If the modulator, which was described by W. J. Rattman, B. K. Yap, and W. E. Becknell of Sylvania Electronic Systems, fulfills its announced capabilities, one of the major limitations of optical systems will have been overcome. This device is supposed to be capable of operation over a 100-MHz bandwidth with less than 10 watts of drive power.

Japanese researchers have recently announced successful construction of injection-laser optoelectronic logic circuits. Optical spectrum measurements indicate that these are potentially capable of logic operation at speeds up to 50 GHz.

VII. WIDEBAND CONTINUOUS RECORDERS

Although this report is primarily concerned with recording of single-transient waveforms rather than with continuous data recording, there have been a number of interesting developments in wideband continuous recorders which may well prove to be of value to us. Such instruments have been developed primarily for radar return processing, television picture recording, electronic intelligence gathering, and recording of telemetry information. Some of these systems record the analog signal directly, while others are digital machines and would have to be preceded by real-time ADC's in order to handle analog data.

The faster systems which have been proposed or constructed all involve some form of laser-, electron-, or ion-beam recording. We shall discuss them in that order. This exposition is not exhaustive, but is intended only to indicate the major areas of endeavor.

The Precision Instrument Company has developed a system called UNICON (Unidensity Coherent Light Recording) which uses an argon laser to burn minute holes in an opaque coating on a transparent polyester 16-mm film. Data are recorded in serial digital form by the presence or absence of the transparent areas, which may be recorded at a rate of megabits per second. The serial data points are laid out in a raster pattern on the film, which is advanced by a helical-scan transport mechanism. The individual holes are approximately one micron in diameter and are separated by a comparable distance. A bit density of 645 megabits per square inch has been achieved. The pulsed laser beam heats up and vaporizes the opaque coating, but the transparency of the backing film permits the beam to be transmitted through the latter without damage. Readout is accomplished by illuminating the tape with a low-power one-micron spot of light and detecting the presence of holes by the electrical output of a photomultiplier tube.

Ampex has developed a system using direct intensity modulation of a laser beam recording on 70-mm positive film. This device may be used for either analog or digital data. For readout a phototube is used to record the intensity of a readout

beam which is controlled by the film density as the film is played back at a lower speed. A tracking system keeps the readout beam centered on the trace.

RCA has developed a related system in which, however, the baseband signal is frequency modulated on a 110-MHz carrier which in turn intensity modulates the laser beam. A number of other concerns have proposed systems similar to those described above.

Minnesota Mining and Manufacturing Company, Ampex, General Electric, RCA, Revere-Mincom, and Eastman Kodak all have constructed systems which use direct electron-beam recording on photographic film. Most of these systems are designed for recording of television pictures, but some specialized systems are capable of analog bandwidths (either intensity modulated or deflection modulated) of greater than 100 MHz. A digital version developed by Ampex is capable of a bit density of 12.5 megabits per square inch, using a 5-micron spot. Several of the systems use a special electron-sensitive positive film developed by Eastman Kodak especially for this application.

One particularly elegant approach uses digital electron-beam writing on film, but the digital information, instead of being written as a presence or absence of the beam or as a step deflection, is written as a modulation at a particular frequency. A lens system then acts as an optical computer operating upon the transmitted light during readout, taking the Fourier transform of the frequency modulated pattern and generating output ones and zeros corresponding to the presence or absence of the correct source frequencies. Obviously this idea could be extended to multilevel digital storage. Optical computing techniques in general have not been exploited adequately.

General Electric, RCA, and Ampex have developed recorders in which an electron beam is used to emboss a thermoplastic film with a conductive backing. The film is softened by heating before recording. Electrons from the writing beam depress the film surface by their attraction to the charged conducting backing. Upon cooling, the depressed trace is fixed in the solidified film surface. A bandwidth of 40 MHz has been demonstrated, and there seems to be no fundamental reason why this could not be extended. Readout is accomplished by a schlieren optical technique.

The Rome Air Development Center (RADC) of the Air Force's Research and Technology Division has a technique for writing binary data on metallic tape using a high energy electron beam. It is reported to be capable of operating at a 50-MHz rate.

The Illinois Institute of Technology Research Institute (IITRI) uses an electron beam to scan a row of tracks on conventional magnetic tape by causing the beam to impinge upon the ends of a row of fine collector wires which pass through the faceplate of an oscilloscope-tube-like vacuum envelope. The other ends of the wires are looped to form a row of miniature magnetic recording heads which span the width of a magnetic tape which is driven past the end of the glass envelope at a high rate of speed. The reading station has a similar row of miniature elementary heads.

Westinghouse has a system called TVIST, an acronym for Television Information Storage Tube, in which an electron beam writes a trace on an insulating plastic film. The film is initially given a surface electron charge by a flood gun. The writing electron beam then discharges the surface locally by releasing free carriers in the body of the film and hence inducing a local conductivity. A related development by RCA leaves a positive charge pattern on a plastic film (rather than a charge depletion pattern) as a result of secondary emission induced by the primary high energy electron beam. This phenomenon is identical to that used for storing a trace on the target of the scan converter tube.

One technique using ion implantation on a plastic film was described by L. R. Bittman at the National Aerospace Electronics Conference in 1962. Positive ions are formed into a broad stream which is normally repelled by a reflector electrode behind the plastic film. When an electron beam is used to write a pattern on the film, the positive charge on the reflector electrode accelerates the electrons to the plastic film where they leave a negative charge pattern. Subsequently, the positive ion stream is used to flood the film and ions can only reach the film in areas where the negative charges have impinged. The number of positive ions

deposited is directly proportional to the original negative charge density, and hence is proportional to the modulation of the original electron beam. Subsequent reading of the film may make use either of an electron beam or of optical techniques.

General Mills, Inc., has demonstrated a Curie-point writing technique closly related to the magneto-optical memory which was described earlier. An electron beam is used to heat a manganese bizmuth film locally to a temperature above its Curie point, at which level it becomes nonmagnetic.. Upon cooling, the state of the remnant magnetic field of the spot is set by an applied magnetic field.

Somewhat slower forms of continuous recorders result from a number of variations of magnetic tape recording. Magnetic drums and discs have been operated successfully at bandwidths of tens of megahertz for both analog and digital recording. Most techniques for increasing the speed capabilities of quasi-conventional magnetic tape recorders involve use of some form of mechanical scanning system to increase the relative velocity between the head and the recording medium. Most of these approaches result either in drastically reduced head and tape life if the head is operated in contact with the tape, or in signal-to-noise ratio problems or varying signal levels (which require frequency modulation) if flying heads are used. One technique which overcomes some of these objections has been developed by M. Camras of IITRI. In this approach a multiplicity of recording heads are scanned electronically in such a manner that the effective recording point on the tape scans rapidly across the transverse dimension while the tape only moves a short distance longitudinally per scan. The resulting direction of magnetization is in the direction of tape motion, as opposed to mechanical scanning systems in which the direction of magnetization is in the direction of mechanical motion, which is transverse to the tape.

Some recent developments in wideband recording are described in the proceedings of two symposia. RADC Report TR-67-325 (Secret) contains the text of the RADC 1967 Wideband Analog Recording Symposium, while the proceedings of the Second Annual Wideband Analog Recording Symposium at the RCA Laboratories, Princeton, N. J., April 30-May 3, 1968, are being prepared for publication as this report is being written.

VIII. SAMPLING RATE CONSIDERATIONS, WAVEFORM RECONSTRUCTION, AND DATA UNFOLDING

The Nyquist principle (that a band-limited signal may be reconstructed completely if sampled at twice the highest frequency of interest) is probably familiar to all who are involved in sampling systems. However, this continuous signal criterion is not completely applicable to sampling of transient waveforms. Sampling of a continuous wave train by a series of short sampling pulses is completely equivalent to amplitude modulation of a pulse train carrier. Such pulse amplitude modulation creates a symmetrical pair of modulation sidebands about the pulse carrier frequency. If the sampled waveform is completely limited to a bandwidth B and the pulse carrier frequency f_c is at least twice the limiting frequency, we have the spectrum situation pictured in Fig. 53a, where there is a clear separation between the upper band edge of the sampled signal and the lower edge of the lower sideband of the pulse carrier. Under these circumstances the original signal may be completely reconstructed by passing the modulated pulse train through a low-pass filter identical to the original filter. The impulse response of such a filter is of a $\sin(x)/x$ form, with the zeros of this function being separated by time increments equal to the pulse period $T_c = 1/f_c = \pi t/x$. Addition of this train of $\sin(x)/x$ responses, weighted by the heights of the signal samples (a convolution process), results in the original waveform. The characteristic $\sin(x)/x$ impulse response extends into negative time (relative to the time of the sampling impulse), and hence implies a noncausal relationship in which an output is detected before the sample has been taken. This nonphysically realizable situation arises because of the nonrealizable perfect band-limiting filter which was assumed at the beginning. The inverse Fourier transform of a perfectly band-limited signal must of necessity lead to a non-time-limited impulse response. If, however, a physically realizable filter with a finite rolloff slope were used, some overlapping of the high end of the signal band with the low end of the lower pulse carrier sideband

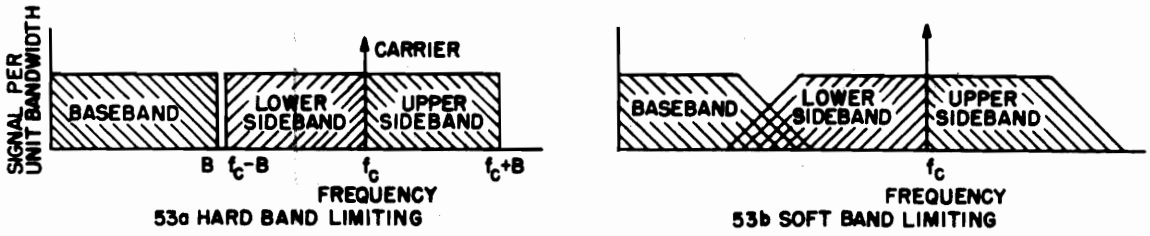


Fig. 53. Spectrum of sampled band-limited signal.

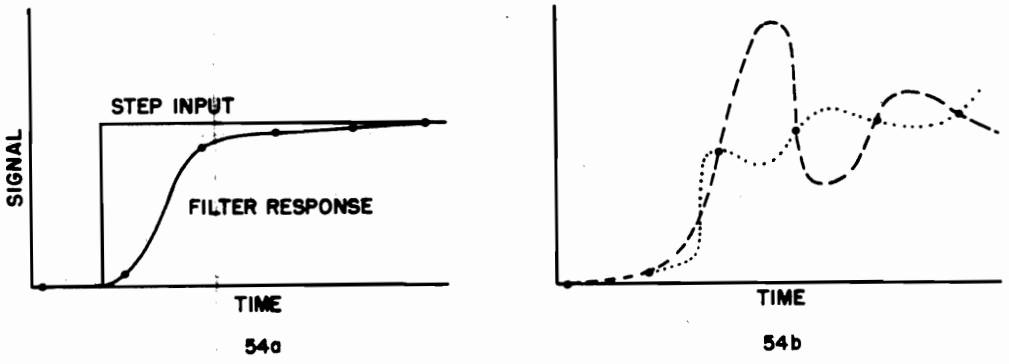


Fig. 54. Sampling of step function input.

must take place as in Fig. 53b, with attendant aliasing distortion of the signal. Even under these circumstances a baseband signal which had no components whatsoever in the overlap region (such as one composed entirely of sine waves) would lead to no aliasing problem.

The very fact that we are interested in recording transients, and thus are dealing with signals of finite extent in time, means that the frequency transforms of these signals cannot be of finite extent in the frequency domain. The combination of physically realizable filters with non-band-limited signals means that the data of interest to us must, of necessity, exhibit aliasing, regardless of whether we sample the signal in real time in some form of ADC, or whether we store the analog waveform and digitize it upon playback for use by the computer. There is no way in which subsequent computer operations can be used to eliminate this effect. However, the degrees of aliasing and signal distortion decrease monotonically as we increase the sampling frequency.

It is common to assume that the frequency at which the response of a low-pass filter is down 3 db (the half-power point) is the upper bandpass limit, and that sampling may be performed at any frequency above twice this value. More careful workers allow an additional factor of 1.5 to 5 (f_c = 3 to 10 times B) to account for the finite rolloff rate of practical filters. It is a very straightforward matter to establish why such factors are necessary. Assume first a desired system resolution of 7 bits (1% or 40 db) and a simple second-order critically damped low-pass filter with natural frequency ω_o and damping constant $\alpha = \omega_o$. The 3-db point of such a filter occurs at $\frac{\omega}{\alpha} = 0.618$, but for 1% resolution the aliased frequency components must be down 40 db, which occurs at approximately $\frac{\omega}{\alpha} = 10$, or a factor of 16 above the 3-db point. This would require an unacceptably high sampling frequency for the signal bandwidths of interest in this report.

A fourth-order filter equivalent in response to two cascaded second-order systems would have a 3-db point at $\frac{\omega}{\alpha} = 0.36$ and a 40-db point at approximately $\frac{\omega}{\alpha} = 3.2$, or a factor of 8.9 above the half-power point, which is not so far outside the range of practicality. More sophisticated filters can improve upon these figures somewhat.

When one is pressing the state of the art to construct a system which is capable of working at all (let alone considering the niceties), the practical manifestation of the considerations described above is as follows. A common rule of thumb is that the 10% to 90% step-function risetime of a low-pass filter (or of any system which acts like such a filter) is approximately one third of the period of the 3-db frequency. Thus, a converter working at a word rate of three times the nominal bandwidth will take samples at time spacings equal to the risetime as sketched in Fig. 54a, where for convenience the samples are shown as occurring fortuitously right at the 10% and 90% points. Only two sets of information are available to the computer for use in reconstruction of the original waveform, which in this case is assumed to be a perfect step. One is that the original signal had the values shown at the sample times. The other is that the system filter has a certain impulse response. The best the computer can do is to convolve (fold) these two sets of information to generate an approximation to the input transient waveform. There is, however, no information whatsoever available to the computer about the behavior of the signal between the sample points shown, with the result that the family of curves sketched in Fig. 54b are equally valid possibilities for what the input may have been. The only factor which makes sampling recorders worthy of consideration at all is some a priori knowledge of the spectrum of the phenomenon being recorded, i.e., the knowledge that independent physical factors will prevent the event being studied from exhibiting wild oscillations with rates or amplitudes greater than one has anticipated and for which one has made provision by selecting a particular sampling frequency.

The sampling rate which a given recorder is capable of achieving is less likely to be determined by the rate at which the sampling gate can be driven than by the limitations of the ADC. The faster types of ADC's described in Section IV involve the use of operational amplifiers, absolute-value circuits, voltage followers, etc. When these are being pushed to the limit, two factors become dominant in limiting the conversion rate. One is

the circuit settling time, i.e., the time required for the circuit to respond to a change in input and to settle to the new value within the required accuracy, which is usually the resolution of the system, or half of the least significant bit. Because of the possibility of ringing in the response of an amplifier working at high frequencies, the final value may be approached either from above or from below. A closely allied phenomenon is slewing-rate limitation. When a circuit is subjected to a sudden change in input, it can only attempt to follow the input rate of change at some maximum slewing rate. Typically this is the result of the active devices only being able to supply some maximum current i_m for charging up the stray capacitance C_s, and hence the maximum rate of change of voltage is i_m/C_s. Only after the circuit has slewed to approximately the new signal value can the active devices return to their linear ranges of operation and start the (preferably nonoscillatory) settling procedure. The sampling rate, and the corresponding input filter bandpass, must be set to allow for these factors or the apparent resolution capability of the ADC becomes a farce. Ideally, of course, the sampling rate and filter are chosen initially to be compatible with the waveforms to be recorded, and then the circuits are designed to have the appropriate slewing rate and settling time capabilities.

When the sampling rate is limited to a lower value than is desired, sometimes more sophisticated sampling approaches can be used in lieu of brute-force high speeds. J. J. Baremore and H. M. Barnard of the Sandia Laboratories have proposed a slow-sampling technique based on signal theory, which offers promise for characterizing a signal sampled at less than the optimum rate. Their technique uses parallel processing of samples not only of the signal itself, but also of samples of the signal passed through filters designed to generate coefficients of an orthonormal set of positive exponential functions. This approach, while requiring considerable additional equipment complexity, appears to offer promise for cases where there are unusual sampling rate limitations.

Three simple approaches are frequently used to reconstruct acceptable approximations to the signal for observation by human beings e.g., on a slow-speed playback oscilloscope. The simplest is a boxcar circuit (a variation of an S&H), which merely holds the value of each sample until the next sample arrives, with the resulting display being a stairstep fit to the waveform. The next more sophisticated playback circuit generates a linear interpolation between the sample points, and hence presents a straight-line segment approximation to the signal. A better approach is to pass the samples through a low-pass filter which has the same relative amplitude and phase characteristics as the original recorder input filter, but scaled down to the playback speed.

Once the waveform is in digital form, the range of possibilities for additional processing is almost unlimited. One of the most important operations is unfolding, which is a process of correcting the recorded waveform for any response-limiting portions of the overall recording installation and sensors, through a knowledge of the measured response of the channel to a well-defined reference function such as an impulse or a step function. Unfolding derives its name from the Faltung integral, or convolution integral. Let the response of a system to a unit impulse (infinite height, zero time width, and unit height-time area) be the the function of time $g(t)$. Then the response, and hence the recorded waveform $F(t)$, of any other input waveform $f(t)$ which starts at zero amplitude is

$$F(t) = \int_0^t f(\lambda)g(t-\lambda)d\lambda \qquad (13)$$

where λ is a dummy variable of integration. If the recorded waveform $F(t)$ and the impulse response $g(t)$ are available, the solution of this integral equation yields the original waveform. This process is called unfolding. Solving this equation under practical circumstances is no simple problem, but several successful approaches are now available.

To obtain the system response, two techniques are available. The first is to use a similar equation. A test pulse $x(t)$ is recorded on a superior recording system and is also applied to the system under test, yielding a recorded waveform $y(t)$. Unfolding these two signals yields the transform $g(t)$, which is then available for unfolding the recorded waveform $F(t)$. Since an impulse function is the time

derivative of a step function, and step functions are more suitable test signals, the latter are usually used and the appropriate computer operations are performed during the unfolding operation.

The second technique makes use of the fact that the inverse Fourier transform of the system complex frequency response is the system impulse response. Both the amplitude-frequency and phase-frequency characteristics of the system are measured, and from these the impulse response is calculated for use in the solution of the Faltung integral. Alternatively, the recorded waveform may be Fourier analyzed, the resulting frequency spectra corrected using the system frequency response, and the inverse Fourier transform taken to yield f(t).

Most unfolding techniques have been optimized for correcting data from systems with degraded high-frequency response, and many of these techniques are not suitable for high-pass systems or those using low-frequency de-emphasis filters. There are, however, a few codes in use which either do not care or are optimized for the latter systems.

IX. SPECIALIZED RECORDERS

There are two specialized types of recorders which do not fit readily within the framework of the discussion presented so far, but whose applications and recording techniques are sufficiently closely related to the aforementioned to justify their inclusion here. The first group are the waveform analyzers, i.e., instruments which examine the waveform for particular features of interest and then record these features, rather than simply "memorizing" the complete waveform. The second group are those recorders which compile a relatively small amount of information about each of a vast array of separate signal sources, rather than recording detailed information about a single source.

A. Waveform Analyzers

A waveform analyzer can only be used where there is an appreciable a priori body of knowledge about the characteristics of the waveform to be recorded. Such an instrument may be required where an appreciable saving in the total amount of information to be recorded can be achieved by making use of this knowledge, thus requiring the recording of only those salient features of the waveform necessary to distinguish between many possible members of a family of related patterns. Typical salient points would be the waveform peaks (both positive and negative), the zero-axis crossings (with their associated slopes), the maximum positive or negative slopes encountered, and any inflection points (zero slopes preceded and followed by slopes of a single sign). Of vital importance to the design of such an instrument are the questions of (1) whether the only requirement is for establishing the existence of such features, or whether one must also know the sequence in which they occur, and (2) whether specific measurements of the times of these occurrences are also required. As we shall see in discussing how these particular features may be detected, it is also of vital importance to have advance knowledge of how many of each type of feature or behavior may be expected to occur in a given waveform.

There are numerous ways in which each of the salient characteristics may be detected or measured, but just a few of these will be discussed here. The magnitudes of pulse peaks of either polarity may be measured by the simple expedient of charging capacitors through diodes of the appropriate polarities, and subsequently submitting the stretched peaks to an ADC. Detection of the mere existence of peaks and/or the times at which they occur may be accomplished by noting that there must be a change in sign of the derivative of the signal at this point. All that is required, therefore, is to supply an electronically obtained derivative of the waveform to an axis-crossing comparator. Where there may be several peaks occurring in succession, some form of commutator is required. An axis-crossing comparator is also the obvious device for detecting zero crossings of the waveform itself, and diode detection of the polarity of the output of a differentiator can establish the sign of the slope at the same point. The slope output of the differentiator may, of course, be sampled with a conventional sampler at this time if the magnitude of the slope is required as the signal crosses the zero axis. The maximum slopes of the waveform may be determined by feeding the output of differentiating circuits to peak detectors identical to those used for recording the peaks of the waveform itself. Inflection points are the most

difficult to measure of the characteristics which have been mentioned. The most promising approach is to make use of the second derivative of the waveform, but this has a tendency to lead to signal-to-noise ratio problems because of the emphasizing of high frequency noise by differentiators.

The most elegant technique for describing a waveform is to use circuitry which generates coefficients of orthonormal sets of functions which may be used for subsequent waveform reconstruction. The problem here is one of optimization, since the most appropriate set of orthogonal functions must be selected for each class of possible waveforms. There is a vast body of literature describing mathematical techniques for selecting appropriate sets of functions, but there is a dearth of proposals for implementing these techniques electronically. The Baremore and Barnard scheme mentioned in Section VIII is one such example.

B. Multiple-Source Data Recorders

The problem of collecting data quasi-simultaneously from many separate points in space is closely related to the recording of successive time points on a single waveform, since in the former case one of the more common techniques is to assemble the data points into a succession of points spaced in time, either for processing or for transmission, and then to reconvert these to a matrix of points separated in space for subsequent submission to a computer. Assuming that each of the separate data signals appears at the recorder on a separate coax, the design problem may be resolved into these questions: (1) What information is required about each of the waveforms? (2) In what sequence do the individual signals arrive at the recorder? and (3) Is it required that the time sequence be measured? We shall sidestep the question of recording a complete time history of each of the waveforms, since this question simply reduces to use of a large number of the types of waveform recorders which have been discussed throughout the body of this report. The more elementary pieces of information which may be required are found in the list of features which could be studied by the waveform analyzers mentioned above, i.e., pulse amplitudes, widths, areas, polarities, and presence or absence of detailed structure. The individual numbers associated with such measurements may either be quantized using any of the ADC schemes discussed earlier, or simply stored as analog values for subsequent transmission to a central data-gathering point.

One of the more vital questions in the design of such an instrument is whether the various data sources generate pulses simultaneously (in which case delay lines or some such means must be used to assemble them in a known sequence), or whether they may occur at arbitrary times (in which case a system is needed for sorting them out, in order to attach identifying "tags" to them). If individual measurements of the times of occurrences of the signals (or some particular characteristic feature on each signal)are required, the problem can become immensely complex. The one approach which seems to have much merit for this quandry is to use a continuously running counter which may be interrogated by a pulse from a decision-making circuit which is sensitive to the particular data pulse characteristic of interest. The resulting times, expressed in binary form, are then stored in a memory which has a particular word address associated with each of the input data cables. Since readout of the contents of the clock register may be difficult to accomplish during a single clock pulse without interrupting the operation of the clock, it probably would be necessary to incorporate a number of slave clock registers, each indicating the current state of the clock, with some form of queing circuit to direct individual decision generators to the available clock registers.

X. SUMMARY

In a search for new techniques for transient waveform recording for use in situations where application of the conventional oscilloscope-camera combination is not feasible, we have studied the recording process in fundamental terms, indicated avenues to be explored, pointed out new devices and technologies which could be applied, and outlined progress made on this and related problems in the recent past. Of the numerous approaches and techniques which have been discussed, only a few have emerged as appearing to be suitable for active pursuit.

The two devices which are potentially capable of achieving the highest frequency of operation, but which also are the most "far out", i.e., not likely to be developed fully within the next three years (even with more active funding), are the solid-state equivalent of the scan converter and injection-laser optoelectronic logic circuitry. The solid-state scan converter would accept the transient waveform signal input on one pair of pins and a sweep voltage (or clock pulses) on a second pair of pins, and store an analog trace as a change of state of the elementary domains of a non-ordered memory plane. Internal or external digital circuitry would supply an output in binary form. The injection-laser logic would be combined with analog comparators and would function more in the nature of a computer operating on the comparator outputs than as a classical recorder.

Recorders which offer promise of development within the next one to three years would be, in decreasing order of desirability, the oscilloscope on a chip, the solid-state ADC with solid-state memory, and the solid-state ADC with a magnetic thin-film memory. Depending upon the economic motivation of the large-scale integration semiconductor manufacturers, the oscilloscope on a chip might actually be constructed, as implied, on a single substrate, or might be a hybrid assemblage of a number of integrated subassemblies. Solid-state ADC's appear at this writing to be completely feasible, with the only question remaining being how far the frequency response and the amplitude resolution can be pushed simultaneously. Solid-state memories for use with these ADC's should become available shortly because of the need for high-speed shift registers for computer scratch-pad memories. In the interim, these can be constructed of discrete components, and limited in size only by the patience and determination of the user. Thin-film memories for use in the same application already exist, and only minor advances are required to push their speeds appreciably higher than those of existing units.

The approaches which appear most promising for construction of fast ADC's depend upon whether they are to be constructed of discrete components or as integrated circuits. The sequential Gray code ADC appears to be the most promising for immediate construction of a discrete-component device combining the maximum currently possible frequency response and resolution. The comparator bank and multilevel-digital-to-binary converter approach would appear to be more promising for a large scale integrated circuit.

For cases where radiation hardening is a prime consideration, the most promising immediate approach appears to be comparators using thin magnetic films or majority-carrier semiconductor devices such as tunnel diodes or UHF field-effect transistors, combined with conversion matrices and memories constructed of the same classes of devices.

The scan converter as presently conceived is the most promising device for immediate application where gigahertz bandwidth and fine resolution are required, and where its bulk and large amount of associated electronic circuitry are acceptable.

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