EMP Interaction Notes

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Some Notes on the Prediction of Generalized/ Transient-Susceptibility Thresholds of Circuits

G. E. Morgan

Autonetics

Anaheim, California 92803

SOME NOTES ON THE PREDICTION OF GENERALIZED/ TRANSIENT-SUSCEPTIBILITY THRESHOLDS OF CIRCUITS

I. INTRODUCTION

With the increasing complexity of military weapon systems has come a need for a deeper understanding of the responses of these systems to electromagnetic transients. Whether the transient is caused by lightning, electromagnetic interference from nearby commercial or military emitters, or other sources, it is becoming increasingly important to understand, in a very detailed sense, the specific characteristics of the system which govern its response to electromagnetic stimuli.

To achieve the desired degree of understanding of system responses to transient excitation, it is essential that an equivalent electrical model be developed which will allow accurate analytical simulation of the entire system to be performed for any given arbitrary input. Only with the development of such a system model, and experimental verification of its adequacy, can the system understanding be raised to a sufficient level to predict responses of the system with a high confidence.

In the most general sense, it is believed these complex military weapon systems can be divided into three parts as is illustrated in Figure 1. It is apparent, however, that depending on the level of the input transient, the antennas and transmission lines could become non-linear (by arcing, for example) and that the "non-linear" circuits might behave in a linear way for small signal inputs. Within a given system there may be many antennas and transmission lines, some of which may be mutually interacting by means of cross-coupling of various kinds. The circuits are highly-complicated, mutually interacting networks of active and passive electronic elements. These, the circuits, are the principal area of interest in the discussion that follows.

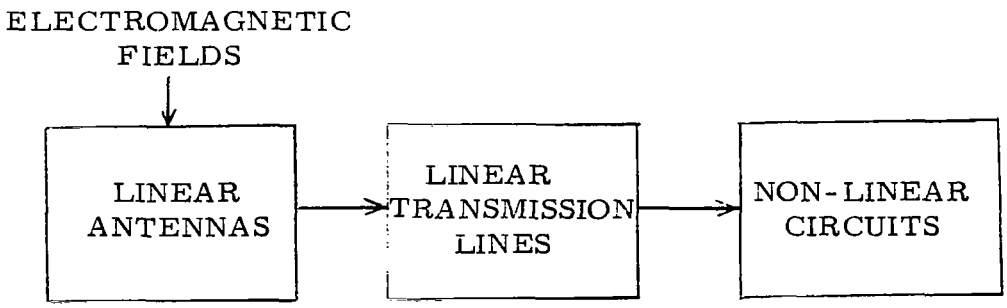

Figure 1. BASIC SUBDIVISIONS OF COMPLEX ELECTRICAL SYSTEMS

This brief note poses more questions than answers. It is offered, nevertheless, in the hope that it will stimulate the thoughts and comments of others in a way that will aid in better defining the problem at the outset. It is, of course, of prime importance to properly define the problem before a solution is attempted.

II. DISCUSSION OF TECHNICAL PROBLEMS

The problem to be considered here is one of methodology; that is, for circuits within a system which are deemed critical. How can the degree of susceptibility be quantitatively defined? More specifically, it is desired to define this threshold in a perfectly general way, independent of waveform so that for any arbitrary transient a judgment can be made as to whether or not the circuit is disturbed functionally.

SYSTEM SEPARABILITY

One of the first questions which must be answered before the study can even begin is whether or not the circuits can legitimately be separated from the associated antennas and transmission lines. If the circuit impedances behave as highly non-linear loads for the transmission lines it is conceivable that a strong interaction may exist between the two which would render invalid any independent analysis of each part separately. It is possible this question might be approached economically by modeling a set of typical transmission line equations on an analog or digital computer and simulating different kinds of non-linear terminations on the line. The question to be answered would be whether or not the overall system behavior can be predicted by an understanding of the characteristics of the individual parts.

For many of the digital circuits two important circuit states will exist; that is, the circuit may be either in saturation or cutoff. This suggests the circuit, although non-linear, may present to the transmission line either a moderately high or a moderately low impedance, depending on the state of the device. In these cases, the circuits might be considered as having two different, but nonetheless linear, states.

If analysis can demonstrate that the non-linear circuits are in fact separable from the transmission lines for the purpose of analysis, then individual circuits can be independently tested in the lab or modeled on the computer to predict quantitative thresholds. If the two prove inseparable, then lumped-parameter models of transmission lines (or distributed models) must be included in computer and/or laboratory simulations. It is essential that this question be resolved early in the study.

Arguments can be made for and against system separability, but it might be noted here that for circuits with a functional threshold, which occurs at low levels, the system may be essentially linear up to the threshold level. What happens above this level may only be of academic interest.

OPTIMUM THRESHOLD-INTERFACE LOCATION

Another important question that arises is where, within the system, is the optimum point where a threshold can be defined. In this, there are at least six possibilities:

1. At each critical node[1] within the topology of the circuit
2. At the circuit interface (inputs, outputs, power, ground, etc.)
3. At a module interface level (module connector, for example)
4. At a black-box or drawer level (interface connectors, for example)
5. At the subsystem level (rack level, missile section, etc.)
6. At the system level (weapon system penetration point, for example)

In contemplating these alternatives, something of a paradox appears. If laboratory or field tests are contemplated, the natural tendency seems to be to start at the bottom and work up the list. If analysis is contemplated, the natural approach seems to be to start at the top and work down.

If correlation of laboratory results with analytical results is contemplated, the choices are narrowed somewhat. That is, it is virtually impossible to make critical node measurements inside integrated circuits; it is nearly as difficult to make measurements at the integrated-circuit interface level in compact airborne equipment; even measurements at module interfaces in airborne equipment would be difficult. Thus, there is a tendency to settle on levels (4), (5) or (6) in airborne electronics and (3), (4), (5) or (6) for operational ground equipment (OGE).

As noted earlier, analysis to define thresholds tends to start at the critical circuit level. In many cases, it is anticipated the circuit problem can be reduced to a particular integrated circuit (IC) deemed critical. Analysis has the advantage that it is probably the best way to really understand what happens to the circuit inside the IC. It is also probably the only way to seek out the critical node, or nodes, within the device. (At this point in time the existence of a critical node in each circuit is merely a hypothesis but, if true, could greatly simplify the analysis effort).

If the IC is to be modeled and analyzed to determine what effects are induced by transients, a problem immediately arises regarding the point-of-entry of the transient into the circuit. Many points exist for most circuits

[1] A critical node is defined here as a single circuit network node whose voltage critically controls or governs the threshold behavior of the entire circuit.

(points-of-entry into a circuit will henceforth be called ports). A typical circuit might have a variety of ports including:

1. Signal input(s)
2. Signal output(s)
3. Power input(s)
4. Ground(s)
5. Synchronizing or clock pulses

These various inputs are illustrated in Figure 2 for a typical flip-flop circuit. Some circuits may have many more ports.

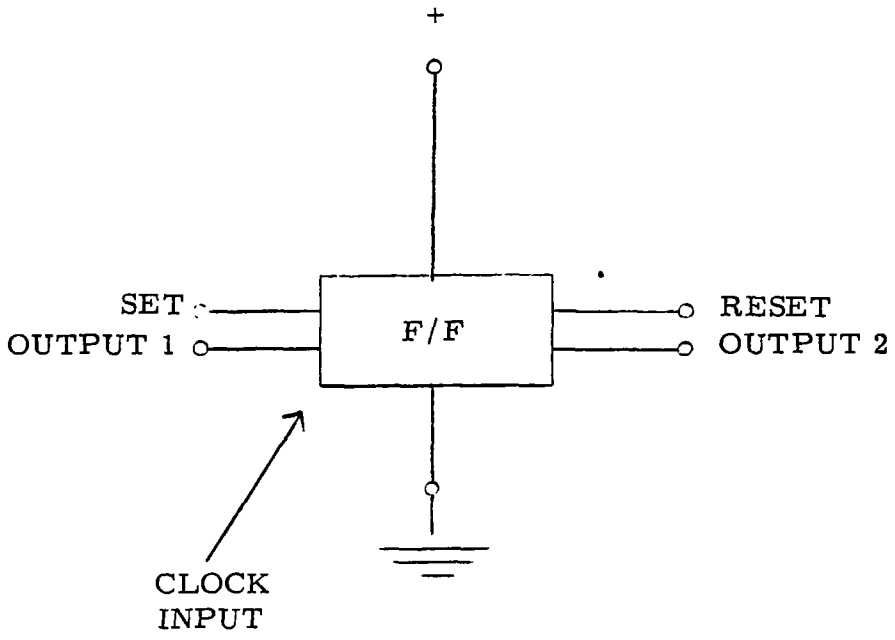

Figure 2. TYPICAL PORTS FOR A SINGLE FLIP-FLOP CIRCUIT (SEVEN-PART NETWORK)

Considering the digital flip-flop circuit as an example, seven ports might be excited simultaneously by an arbitrary transient. The transient waveform at each input port might be different, depending upon how it got there. If the precise waveform were known at every port, the response of the circuit could be computed with ease; no new methodology would be required. But if all are excited simultaneously by arbitrary waveforms the definition of a threshold gets somewhat nebulous. If one single critical node (or even two critical nodes) can be identified within the circuit then the effect of each port on the voltage at that critical node would be of considerable interest. It is

possible that linear superposition might apply, although it may not. In at least one flip-flop previously studied (in one airborne computer) signals at the SET port could inhibit the response of the RESET port or vice versa. That is, this flip-flop was highly resistant to double triggering. This was true even for production hardware where transistor betas were considerably different for the left and right sides of the circuit. The point here is that some ports may inhibit others, possibly in a non-linear manner, and that it is simply not adequate to select arbitrarily one or two ports for signal injection and assume no other ports are excited; in fact, it is almost intuitively obvious that more than one port will be excited.

If a critical node can be proven to exist within a given circuit and if the number of circuit ports is not great, it may be possible to apply matrix methods to the description of the circuit; that is, to relate the signal at the critical node to the instantaneous signal at each of the circuit ports if the circuit is linear.

Since this appears rather difficult, there is a tendency to look for an easier way (See Figure 3). If the problem is viewed from the next higher assembly level (the module), the problem is seen to be even more complicated by the large number of connector pins usually in the module; also because these connectors are relatively close to the circuit each pin would have to be driven by the proper waveform to determine the correct circuit threshold - an obviously formidable task.

In further pursuit of simplicity at even higher levels of assembly the black-box (or ground equipment drawer) might be considered next. At this level the number of individual wires is often very large but they are grouped into cables; if the incoming transient can be shown to be primarily a common node signal (and it often is) then each cable can be treated as one port in which all wires can be simultaneously excited by one common mode, bulk current driver. Viewed in this way a black-box or drawer level may actually be simpler than the module or circuit level, particularly if there are only a few cables feeding that assembly. If these cables are a considerable distance from the point of entry (POE) of the energy into the weapon system and not too close to the circuit, there is even some logic in assuming the transient on each of these cables is similar in waveform, suggesting the feasibility of obtaining approximate thresholds by driving each of these cables with the same waveform simultaneously. Of course, it would be better to drive each cable simultaneously with a careful simulation of the proper waveform once the proper waveform is known, but prior to that time other approaches may be required.

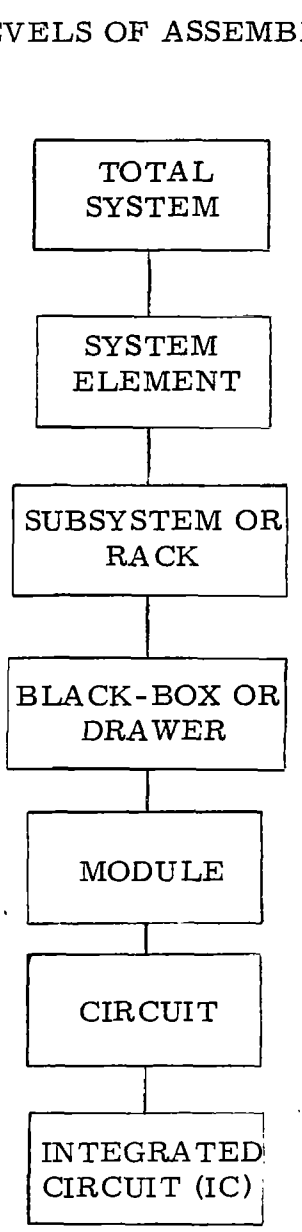

Figure 3. GENERALIZED LEVELS OF ASSEMBLY

Regarding the difference between common mode and differential signal injection, it is assumed here that the type of excitation must be identified at, or near, the point of weapon system penetration. If differential modes are dominant then each excited signal pair must be identified at the penetration point and traced out to each affected subsystem where it can be treated separately. If a differential signal pair gets separated into different cables within the system there is some reason to believe all nearby wires in these cables

will take on a common mode signal similar in character to that carried by the isolated leg of the differential pair. Thus, even differentially induced signals may ultimately appear as common mode signals at critical circuits.

Climbing to still higher levels of assembly in the pursuit of simplicity, the next logical level might be the missile section (containing several to many black-boxes) or the ground equipment rack. In general, these levels of assembly tend to have fewer (but larger) cables than the sum of all black-box or drawer level cables inside which offers some further advantage. The ports at this level are sufficiently distant from the circuit to allow "good" simulations of waveform at the critical circuit to be produced by "less than good" simulations of the rack interface driving signals. At this level of assembly it is sometimes possible to excite all critical circuit ports in just the right proportion by driving only one port at the rack or missile section. It has the further advantage that many circuits are excited simultaneously which aids in the evaluation of subsystem "logic races" (i.e., interactions of various parts of the circuit logic with each other).

If an even higher level of assembly is attempted, such as a total missile, or a total ground system, the problem might get even easier but generally speaking these tests can no longer be performed conveniently in the laboratory so that tests or simulations in the field often become necessary (not always true, of course).

Implicit in the above discussion is the partly intuitive belief that laboratory simulations are most meaningful and often easiest to perform when conducted at a high level of assembly. Some of the logical reasons for this belief are as follows (See Figure 4):

1. If an injection test is performed at the interface level denoted (D) in Figure 4, for example, it tends to avoid the multiport problem associated with interface levels (F), (G), and (H). In other words, injections at level (D) will excite all ports at level (H) almost automatically.

2. In the event the circuit response is significantly influenced by the source impedance of the incoming transient signals, then the point of injection should be as far away from the circuit as possible to encompass as many of the actual system impedance leading to the circuit, as possible. Level (D) may be the highest level of assembly that can be conveniently tested in contractor laboratories and this is an adequate choice for that reason. (At least initially)

3. If the system transfer functions (between specific circuits and the point of signal injection) contain strong resonances at particular frequencies (resulting from relatively low-Q resonant circuits) the waveforms at the circuit level may be primarily dictated by these resonances and may, thus, be less critically dependent on proper waveform simulation

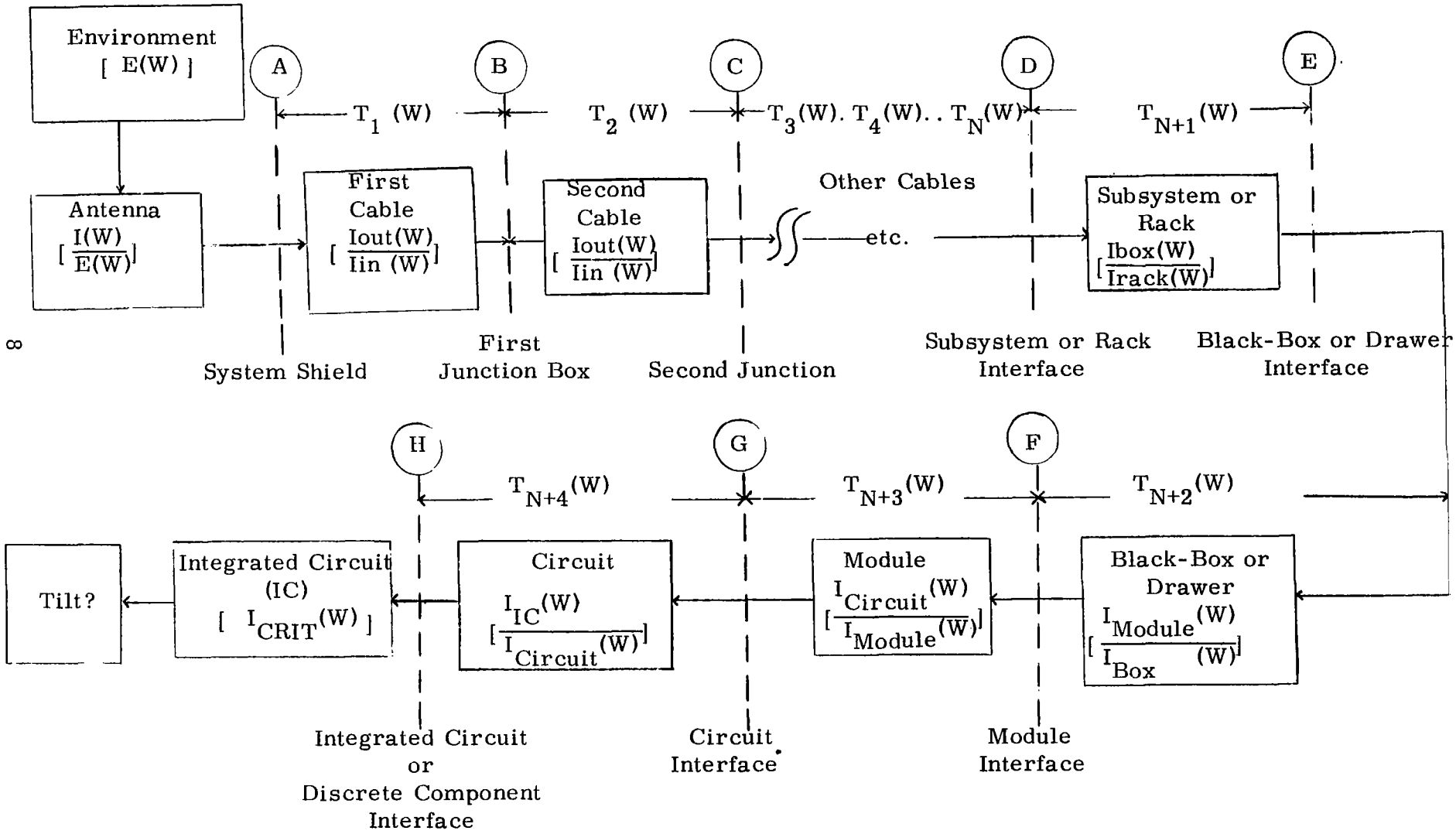

Figure 4. INTERFACES WITHIN A TYPICAL SYSTEM

at the input to the system, particularly if signals are injected at a high level of assembly. This is because the circuit level frequency tends to be dictated by these resonances and the duration is heavily influenced, if not dictated, by the Q of these resonant circuits. To some extent, then, the "proper" circuit level waveform can often be produced by merely shock exciting the system at a high level of assembly with any reasonably good estimate of the expected waveform. This is not believed to be true for most lower levels of assembly and, for these, very accurate simulations of waveform may be required.

4. If the number of critical circuits is large (critical in that these circuits could conceivably cause difficulty) then the task of testing each circuit individually gets very great indeed. By testing at the highest practical level of assembly many circuits can be excited simultaneously and the work required is greatly reduced. A test at the rack or subsystem level also has the advantage that it can lead to a ranking of the critical circuits. Certainly all circuits deemed critical at the beginning of a study are not equally critical. Ranking allows proper priorities to be established for the detailed circuit analyses.

5. By testing large numbers of interconnected circuits at one time the interactions between circuits can also be evaluated.

6. By testing many circuits simultaneously in a large assembly (some of which are deemed critical and some of which are not) problems not foreseen or anticipated can be detected. Certainly past experience with the transient responses of complex systems has clearly demonstrated that not all problems are foreseeable. In fact it is virtually certain that initial lists of critical circuits will be incomplete. Tests at high levels of assembly can detect these oversights.

Thus, it can be seen there are a number of reasons why injection tests at the highest practical level of assembly should be performed early in the investigation.

As a result of the above arguments it appears that there are certain advantages to conducting tests in the laboratory at the rack level or missile section level. Higher levels of assembly can and should be tested probably in the field. In driving a rack or missile section, the initial tests could be or might be, conducted in such a way as to excite all interface cables simultaneously with identical common mode signals pending the identification of important differential signal pairs, if any, and/or obtaining a more precise knowledge of the specific waveforms expected on each cable.

The output of such tests would be a ranking of circuits in the probable order of criticality, better data on which to base measurement lists for field measurements and a prioritizing of circuits for detailed analysis at the circuit level. For this purpose it may also be possible during the rack or missile section tests to measure voltages at each circuit port on selected circuits to obtain approximate input data for the analysis of the circuit as a multi-port network.

This rack level, or missile section, injection test has other advantages. It is a test which could be performed soon using available pulsers. The existing pulsers are capable of generating repetitive damped sinusoidal current pulses of different frequencies and different damping. Early tests would not be designed to define actual subsystem thresholds, per se, since this can only be done by carefully simulating the exact input waveform or by very careful and detailed circuit analysis. Instead, these tests would be used to improve the list of critical circuits and to assure that the proper attenuation is focused on the most critical circuits during field measurements and in-house laboratory tests and analyses.

Useful as such subsystem level tests might be, they are not, in themselves, sufficient. Other tests and analyses should be performed concurrently to begin to examine what goes on at the lowest (circuit) level during a transient event. Some of the problems involved in this investigation are outlined in the sections that follow.

The question to be addressed here is whether or not a generalized circuit level threshold can be defined.

The problem created by the multiport character of even the smallest circuit (such as an IC) has already been discussed including the effect of interactions of different ports.

Another complication that must be considered is whether or not the circuit threshold is highly waveform dependent. Some circuits are known to have this characteristic. One mechanism by which this takes place occurs in a circuit which can accept electrical charge faster than it can reject it, that is, given a high frequency input signal the circuit will accumulate electrical charge rapidly on the first half cycle, discharge slighly on the next half cycle, accumulate even more charge on the next half cycle, and so on. The circuit will thus accumulate a voltage over a number of cycles of the waveform and the ultimate threshold effect will depend not only on the magnitude of the input signal but also the waveform. This effect is subsequently referred to as stacking in this report.

Other circuit characteristics may also cause waveform dependence. It appears, for example, that if the circuit contains elements between an excited port and a critical node which together have singularities in the transfer function describing this path, the threshold may also be waveform dependent.

It is believed that many electronic circuits will have short time constants for the frequencies of interest and that these circuits will behave simply as voltage critical devices where the threshold can be best defined at one critical node or even at one particular port. It is important, however, to examine each critical circuit to assure that this is in fact true. If it should develop that many circuits are highly waveform dependent, then the feasibility of defining generalized circuit thresholds (independent of waveform) may be in doubt.

Circuits which stack voltage may be analytically characterized by two time constants, one for charging and one for discharging. But the analytical description of other types of waveform dependence is not apparent at this time.

Based on experience with critical circuits in the past, it is known that circuit thresholds are frequency dependent. Circuit thresholds are often constant up to some frequency, after which they increase. The absolute reasons for this increase are not known for certain at this time but are believed related to distributed circuit reactances, transistor internal capacitances, transistor gain loss, or combinations of these. Some circuit thresholds have proven to be smooth, rather well-behaved, monotonically increasing functions up to 70-100 MHz. It is anticipated, however, that other circuits may exhibit resonant characteristics at some frequency below 100 MHz.

The non-linear effects of circuits on overall system behavior are not well understood. Changes in input impedance at each port as a function of signal amplitude could severely complicate the analysis of system behavior. However, even this complication may not prove intractable. The overall system level threshold is likely to be dominated by a collection of circuits whose thresholds are low. Up to the levels required to upset these circuits, the circuit input impedance changes may not be great. At higher levels what happens may only be of limited interest.

It is assumed implicitly in this that the levels experienced at the circuit level will not be allowed to exceed the circuit damage threshold (as a matter of system design philosophy). In general, it is considered impractical to design each circuit to withstand very large overstresses (sufficiently large to cause junction burnout, wire burnout, semiconductor cracks, etc.). It should also be recognized, however, that at very low frequencies, small junction semiconducting devices could experience junction burnout at relatively low levels. This is not expected to happen often in actual systems, however, because the associated "antennas" which pick up the stray energy are typically very ineffective at very low frequencies (<100 KHz, for example).

Individual circuits may also be non-stationary in that their susceptibility varies with time. This may be true for digital devices which change state at various times (change from saturation to cutoff and vice versa). The susceptibility of the circuit may be different for the two states so both states

PRELIMINARY CRITICAL CIRCUIT ANALYSIS FOR NOMINAL THRESHOLDS

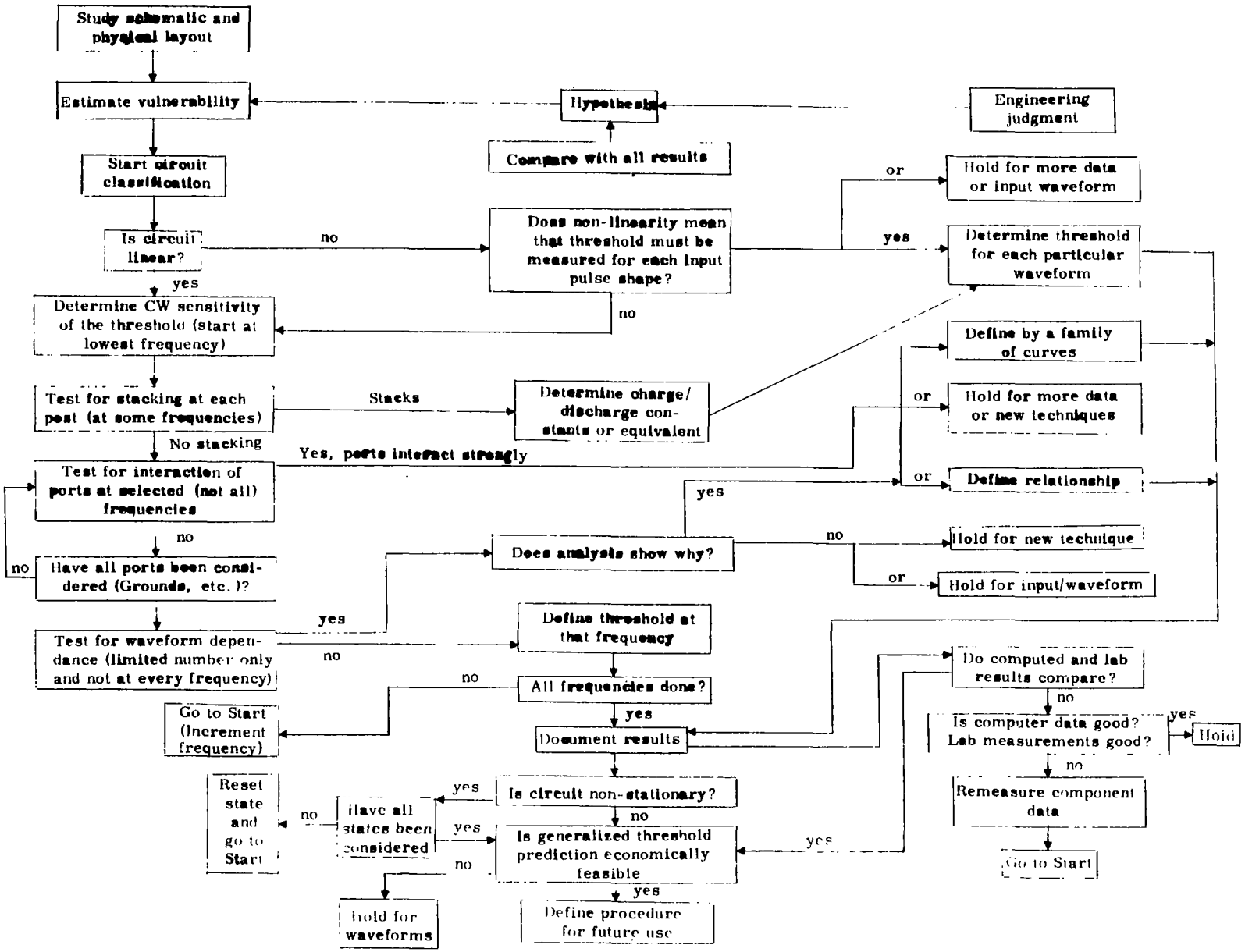

Figure 5.

must be checked. There may also be a few (probably not too many) circuits which have more than two states. Analog circuits with time varying bias might have a wide range of thresholds; in this case it may be desirable to analyze or test the worst case.

The diagram in Figure 5 shows one possible approach to defining the arbitrary generalized threshold of one circuit. It consists primarily of trial and error tests to categorize the circuit prior to specific threshold evaluation. The diagram implies these could be some circuits which defy generalized threshold description at the circuit level. It also indicates that the magnitude of the problem for even one circuit might be considerable.

The problem may not be as severe as this diagram might suggest, however. If the circuit contains only one critical node which dictates circuit thresholds and if only one port couples appreciably to this node, and if the critical node is only voltage level dependent (no stacking or other waveform dependence) then that circuit threshold can be readily defined as one graph of voltage or current versus frequency required to disturb the circuits. It is hoped this may yet prove to be the case most of the time but at present there is too little data at hand to say for certain.

For these reasons, it is believed there is merit in studying a small sample of critical circuits at the isolated circuit level. This will give some clues as to the possible completeness and adequacy of a trial and error method such as Figure 5, will provide some data on the difficulties and costs of the circuit shakedown, will build a data base for use in developing other analytical models of the circuits, or other approaches to the description of a threshold. It will also provide data suitable for correlation with computed circuit responses using available circuit analysis computer codes. The latter is considered very important since the proven ability to compute accurate predictions of circuit thresholds is essential to a real understanding of circuit behavior. It is, as was noted earlier, almost the only way to determine what goes on inside an IC, for example. The feasibility of computer predictions is the subject of the following section.

FEASIBILITY OF COMPUTER PREDICTIONS OF CIRCUIT THRESHOLDS

Relatively few attempts have been made to use computer codes to predict multiport transient responses of circuits at high frequencies, as far as the writer knows. For those cases which have been attempted, the circuit had one port which was believed to be dominant and the predicted threshold for that port checked rather well with laboratory measurements which excited that port up to frequencies as high as 7 MHz. Some circuit computer analyses have departed seriously from lab measurements, however, for frequencies as low as 1 MHz.

Two questions must be examined in seeking better computer predictions. The first of these is whether or not the transistor models used in the

computer program are adequate for high frequency use. The second is whether or not the circuit components are adequately characterized for input to the computer.

The question of which transistor model is best is a debatable one on which differences of opinion exist even among the experts. However, it appears that the difference between the Ebers-Moll and the charge control transistor models is small for frequencies below 10 MHz for most semiconductor devices of interest. In any event the differences are believed to be even less significant when compared to the errors introduced by imperfect characterization of circuit distributed reactances, parasitic transistor effects, and imperfect data on components (transistors, resistors, capacitors, etc., particularly those inside an IC). Computer predictions within a few percent are believed possible if:

1. The component data used for input to the computer is measured with great precision.
2. The laboratory circuit model used to verify the prediction is precisely the circuit modeled on the computer.
3. The laboratory measurement techniques on the circuit are made very accurately.

This has been demonstrated in radiation effects analyses on circuits (TREES type). In showing this high degree of correlation between predicted and measured circuit transient effects, however, it has proved to be a very difficult job involving much hard work and is only practical for demonstrating that the computer program is theoretically correct. Such an approach for predicting transient thresholds in general would appear to be inconsistent with the probable parameter variations from device to device or circuit to circuit (a topic to be discussed in more detail later). With reasonable attention to component characterization at high frequencies, at least up to 10 MHz, it appears that predictions within 10% should be attainable using existing computer programs.

The relative cost of computer analyses versus laboratory tests for defining generalized multiport transient thresholds is not yet known since too few attempts have been made to establish a cost history. It is the writer's opinion that lab tests alone may prove less expensive than computer analysis alone. But, very likely, a combination of the two will provide the best overall understanding at the lowest overall cost.

Certainly obtaining a detailed understanding of generalized transient responses of circuits is greatly aided by the availability of a proven, trustworthy computer code. The effort required to reach this point is not expected to be prohibitive and appears to be well worth priority attention.

The accuracy of laboratory data can be approximately specified by the RMS combination of the individual instrument specified (or calibrated)

accuracies. This could be used to bound the errors for the particular circuit under test but will not, of course, indicate the variations from circuit to circuit.

COMPUTED THRESHOLD DATA

The method for estimating the error associated with computed predictions of thresholds is not obvious. It is believed the error may increase and decrease with frequency. It will depend partly on the accuracy of the input component data and partly on the errors inherent in the transistor model. Errors could, no doubt, be estimated on this basis, but there is some question as to whether this is economically feasible. It may be preferable to perform an error estimating study early in the program to generally define the accuracy of computer program assuming typical component data accuracy. This question needs more study.

VARIANCE OF THE FLEET

It is one matter to bound the errors on a measured or computed threshold for one particular circuit sample or circuit mode; it is a much more difficult question, however, to attempt an estimation of the variance of the many different circuit samples in the fleet. This problem has not really been solved by anyone in the industry as far as the writer knows. It is a question which frequently arises in TREES analysis. It is equally applicable here.

There are, of course, various ways to obtain estimates of the variance of any given circuit performance analytically. One such technique involves the measurement of enough samples of each of the individual components (resistors, diodes, transistors, capacitors, etc.) to obtain estimates of their individual distributions and then to combine these distributions analytically by Monte Carlo techniques (repetitive runs using random samples from the individual distributions). Cost problems appear prohibitive, however, since the measurements would be destructive (integrated circuits would have to be cut open, components isolated by cutting or scribing the interconnect metallization, new wires bonded to each end of the IC "components" and measurements performed). Since individual component values inside an IC are not separately controlled during manufacturing (only overall circuit input/output relationships are controlled) the distributions of the parts inside may be relatively broad which suggests the sample size might have to be large. The added cost of many Monte Carlo computer runs further contributes to the opinion that this approach is probably too costly.

A purely empirical approach might be used instead; that is, a straightforward statistical sampling of the circuits in the fleet might be performed to determine some estimate of the variance of the threshold within the fleet. This implies that a statistically significant sample of circuits from the fleet can be made available for test and that the tests can be conducted efficiently and in a

non-destructive manner (which may be possible, given the knowledge derived from previous engineering threshold tests). The cost of this approach in time, dollars and inconvenience to the fleet may still be prohitibitive. Until more is known about generalized threshold measurements it is difficult to estimate the cost and time.

Short of doing nothing at all with this problem, there may be some other less expensive ways to approach the fleet variance problem. The purely analytic estimation techniques would seem to be marginal, however, for circuits which may be both non-linear and non-stationary. This needs further study.

Probably the Task Working Group should consider whether the fleet variance problem is important enough to warrant any consideration and, if so, what statistical confidence is reasonable for the estimates of the variance. Program directors should then probably be asked to evaluate the feasibility of obtaining samples from the fleet for test, either on-site (as a part of a survey effort) or for off-site tests by various contractors or associates. If the problem is to be considered seriously the optimum technique should be carefully developed to give the best estimate of the variance at the lowest cost within the bounds of the confidence desired.

III. CONCLUSIONS

Conclusions this early in the study are probably premature, but in the interest of initiating discussion of the problems some tentative conclusions are presented below:

1. The generalized description of circuit thresholds is not a trivial technical problem and a proven methodology, for achieving this goal does not presently exist. Nevertheless a trial and error approach appears possible for initial efforts.

2. Neither the computer programs nor the component data presently in existence have been proven adequate for predictions above about 1 MHz. Checking the adequacy of both, however, and upgrading as required is a worthwhile goal and is not expected to be a major difficulty, at least up to 10 MHz. The application of even a proven computer program, however, may not lead to rapid threshold predictions in view of the multiport problem, stacking, non-stationarity and other waveform dependent considerations.

3. The separability of the circuits from the associated transmission lines would appear to depend on the degree of non-linearity of the individual circuit input impedances. But even if these impedances are found to be highly non-linear over the region of interest, it may still be feasible to separate the two if it can be shown that predictions of the

behavior of the combination can be achieved by understanding the individual parts. The approach to the proof of the latter requires further study.

4. Tests in the laboratory should initially be at least of two kinds:

   (a) Rack, Missile Section, etc., injection tests to develop better insight, refine measurement lists, rank circuits, spot unanticipated problems and provide approximate information on the relative magnitudes of signal arriving at different ports of the circuits deemed most critical. These tests can also be used to derive internal subsystem transfer functions for critical internal cables. These tests require very little equipment other than the hardware under test and its checkout gear. Injection pulses, oscilloscopes, current probes (and/or voltage probes) are all that is required. Injected waveforms might initially be damped sinusoids driving simultaneously onto all interface cables. Better simulations can be made as data becomes available.

   (b) Circuit level or breadboard tests to generate data suitable for comparison with computer models. Probably these tests would be most often compared with computer predictions for excitations applied to only one port at a time. The purpose here is to aid in the proof of the computer program and/or the adequacy of associated component data and to obtain more experience and data on factors affecting even single port thresholds and the degree of importance of each. Data can also provide a useful base for testing future theories for thresholds prediction.

5. Supplementary tests in the field are clearly indispensable.

6. Real understanding will only come from a judicious combination of lab tests, computer analyses and field tests.